

UNCLASSIFIED

AD NUMBER

ADB002282

LIMITATION CHANGES

TO:

Approved for public release; distribution is unlimited.

FROM:

Distribution authorized to U.S. Gov't. agencies only; Test and Evaluation; AUG 1974. Other requests shall be referred to Naval Surface Weapons Center, Attn: FVR, Dahlgren, VA 22448.

AUTHORITY

USNSWC ltr, 26 Mar 1984

THIS PAGE IS UNCLASSIFIED

AD B.002282

AUTHORITY: USNSWC Ltr, 26 MAR 84



AD B002282

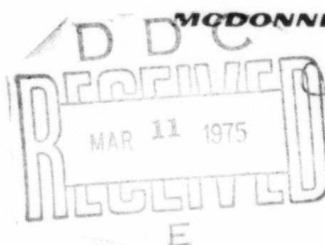
AD No. _____
DDC FILE COPY

(1) MDC E1126
— J

INTEGRATED CIRCUIT ELECTROMAGNETIC SUSCEPTIBILITY INVESTIGATION - PHASE II

SUSCEPTIBILITY SURVEY STUDY

MCDONNELL DOUGLAS ASTRONAUTICS COMPANY - EAST



MCDONNELL DOUGLAS

CORPORATION

5

1

COPY NO. 17

6

INTEGRATED CIRCUIT ELECTROMAGNETIC SUSCEPTIBILITY INVESTIGATION PHASE II.

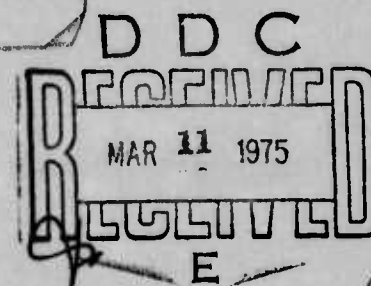
11 9 AUG 1974

14 MDC-E1126

12 74p.

SUSCEPTIBILITY SURVEY STUDY.

SUBMITTED TO:
CONTRACTING OFFICER
U.S. NAVAL WEAPONS LABORATORY
DAHLGREN, VA. 22448
CONTRACT NO. 15 N00178-73-C-0362



MCDONNELL DOUGLAS ASTRONAUTICS COMPANY - EAST

Saint Louis, Missouri 63166 (314) 232-0232

Distribution limited to U.S. Gov't. agencies **MCDONNELL DOUGLAS**
Test and Evaluation; AUG 1974 Other requests
for this document must be referred to

Naval Surface Weapons Center
Code FVR, Dahlgren Lab.
Dahlgren, Va. 22448

403930

PREFACE

This document is one of eight task-oriented reports prepared under Contract No. N00178-73-C-0362 for the U. S. Naval Weapons Laboratory, Dahlgren, Virginia 22448. The McDonnell Douglas Astronautics Company Personnel involved were:

J. M. Roe, Study Manager

J. R. Chott

C. E. Clous

V. R. Ditton

T. A. Niemeier

G. W. Renken

R. D. Von Rohr

J. A. Waite

This report was reviewed by J. R. Cummings.

TABLE OF CONTENTS

<u>Title</u>	<u>Page</u>
1. INTRODUCTION	1
2. DIGITAL DEVICE SAMPLE	3
2.1 Digital Test Plan	3
2.1.1 Susceptibility Threshold Limits	4
2.1.2 Test Setup	5
2.2 Digital Results	6
2.2.1 Most Susceptible Port Results	6
2.2.2 Susceptibility Threshold Levels	10
2.2.3 Multiple Susceptibility Levels	14
2.2.4 Susceptibility Threshold Level Dependence Upon RF Duration	15
2.2.5 Data Correlations	17
3. LINEAR DEVICE SAMPLE	21
3.1 Linear Test Plan	21
3.1.1 Susceptibility Threshold Limits	21
3.1.2 Test Setup	23
3.2 Linear Results	29
3.2.1 Most Susceptible Port Results	29
3.2.2 Susceptibility Threshold Levels	29
3.2.3 Multiple Susceptibility Levels	34
3.2.4 Susceptibility Threshold Level Dependence Upon RF Duration	34
3.2.5 Data Correlations	34
4. COMPARISON OF DIGITAL AND LINEAR TEST RESULTS	37
5. CONCLUSIONS AND RECOMMENDATIONS	41
6. REFERENCES	43
APPENDIX A - DIGITAL SUSCEPTIBILITY LEVEL PLOTS	45
APPENDIX B - DIGITAL SUSCEPTIBILITY LEVEL DATA	57
APPENDIX C - LINEAR SUSCEPTIBILITY LEVEL PLOTS	59
APPENDIX D - LINEAR SUSCEPTIBILITY LEVEL DATA.	71
APPENDIX E - CIRCUIT DIAGRAMS OF DEVICES TESTED.	73
DISTRIBUTION LIST.	79

List of Pages

Title

ii-iii

1 through 83

iii

INTEGRATED CIRCUIT SUSCEPTIBILITY

MDC E1126
9 AUGUST 1974

1. INTRODUCTION

A comprehensive analysis of RF effects in pn junctions has begun on the 7400 quad two-input TTL NAND gate (see "Bipolar NAND Gate Study", Report MDC E1123) and the 741 operational amplifier (see "Bipolar Op Amp Study", Report MDC E1124). The basic RF interference phenomenon for these devices is considered to be rectification at the pn junctions. This survey was performed to provide some assurance that the 7400 and 741 were not "odd balls" with regard to susceptibility levels and effects, to obtain more information on the range of susceptibility levels for various digital and linear devices, and to provide data that can be used to verify analysis techniques derived from the 7400 and 741 studies. RF susceptibility testing was performed on 10 digital and 10 linear devices.

The basic results of this survey indicate linear devices to be more susceptible than digital. The range of susceptibility threshold levels was from 0.000003 to 0.27 watts for linear devices and from 0.0029 to 3.8 watts for digital devices. In general, for digital devices, the output in a logical low state was found most susceptible, and for linear devices, an input (usually inverting) was found most susceptible.

INTEGRATED CIRCUIT SUSCEPTIBILITY

MDC E1126
9 AUGUST 1974

2. DIGITAL DEVICE SAMPLE

Table 1 lists ten digital devices chosen for RF testing and indicates their family type and logical function. These 10 devices represent some of the more commonly-used logic functions available to equipment designers.

2.1 Digital Test Plan - Testing was performed at 0.22, 0.91, 3.0, and 5.6 GHz with devices operating under normal DC bias conditions. A sample size of 5 was used for testing of each device type. For purposes of this investigation, the most susceptible RF entry port and DC test configuration were determined through RF testing at 3.0 GHz and then used throughout testing at all frequencies.

Table 1 DIGITAL DEVICE SAMPLE

DEVICE NUMBER	FAMILY TYPE	LOGICAL FUNCTION
7432	TTL	QUAD 2-INPUT OR GATE
7402	TTL	QUAD 2-INPUT NOR GATE
7404	TTL	HEX INVERTER
7405	TTL	HEX INVERTER (OPEN COLLECTOR)
7450	TTL	EXPANDABLE DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE
7473	TTL	DUAL TYPE J-K FLIP-FLOP
7479	TTL	DUAL TYPE D FLIP-FLOP
3021	TTL	QUAD EXCLUSIVE OR GATE (HIGH SPEED)
4011	CMOS	QUAD 2-INPUT NAND GATE
2002	HYBRID	HIGH POWER DRIVER

In previous work, interference RF testing was performed by recording the dissipated RF power and the resulting RF effects over a wide range of RF power. This produced a smooth curve of RF effects versus dissipated RF power. From these curves, the effects of RF power at any level within the testing range can be easily obtained, and comparisons among devices can be made at any desired RF power level. For this study, however, arbitrary interference levels were defined based upon normal use patterns. Measurements were made at zero RF power, maximum available RF power, and two points between. One of the intermediate points was made at the power level required to produce the defined output voltage (susceptibility threshold) in order to make comparisons among devices. The limits used are described in the next paragraph.

Previous results on the 7400 and 741 had shown limited temperature effects, but prudence requires continued care when relatively high levels of power are being dissipated in the chip. Accordingly, a 500 μ sec pulse was used to find the susceptibility threshold (most temperature effects require more than 500 μ sec to manifest themselves). For completeness, temperature effects were noted when detected, but it was beyond the scope of this study to carry out a detailed investigation in this area.

The most susceptible port was considered to be that port which, when subjected to RF power at 3.0 GHz, resulted in the output voltage exceeding a susceptibility threshold level at the lowest level of RF power dissipated in the device.

2.1.1 Susceptibility Threshold Limits - The acceptable output voltage range for the logical high and low states of the 7400 series devices is depicted in figure 1. The functionally acceptable range for a logical "zero" or low state output voltage is $0 \text{ volts} < V_{out_{low}} < 0.8 \text{ volt}$. Since the maximum input voltage a 7400 series gate is guaranteed to recognize as a low level is 0.8 volt, the 0.8 volt level was chosen as the susceptibility threshold for these tests. Device inputs have internal protective diodes which clamp negative voltages appearing at the inputs to

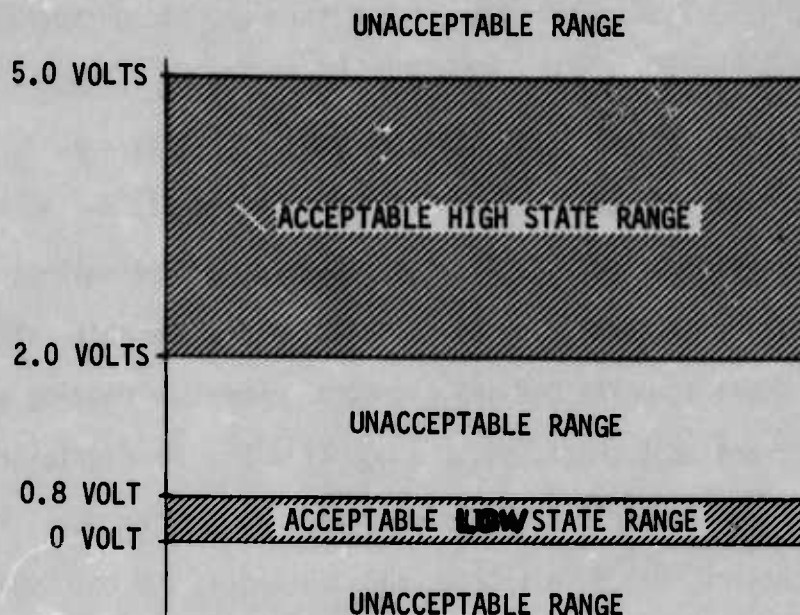


FIGURE 1 LOGICAL LOW AND HIGH STATE OUTPUT VOLTAGE RANGE

approximately -0.6 volt. In order not to damage these protective diodes through interference testing, a 0 volt lower limit was chosen as the minimum low state output susceptibility threshold level. The 7400 series functionally acceptable range for a logical "1" or high state output voltage is $2.0 \text{ volts} < V_{out_high} < 5.0 \text{ volts}$. The minimum input voltage a 7400 series gate is guaranteed to recognize as a high level is 2.0 volts, so 2.0 volts was chosen as the susceptibility threshold for these tests. The absolute maximum high input allowable is specified to be 5.5 volts. In order not to damage the input during interference testing, a 5.0 volt upper limit was chosen as the maximum high state susceptibility threshold. These chosen limits are not intended as absolute levels of interference for the design engineer. They are simply levels chosen to perform all digital tests to allow comparisons of data. CMOS and hybrid susceptibility limits were similarly chosen based upon manufacturer specifications. For more on CMOS and hybrid testing and results, see reference 1.

2.1.2 Test Setup - While changes in the output voltage are used as an indication of RF interference, all other device parameters can be affected by RF. In general,

proper output voltage response to input conditions may be considered the most important parameter of operation. However, changes in other device parameters can also significantly affect a circuit's operation. Therefore, DC voltage, DC current, and RF power are monitored at all device terminals during RF testing. Due to the large amount of data collection required, a semi-automated test system was devised. Testing is controlled by an HP 9810A programmable calculator which operates a 50-channel scanning DVM and cassette memory for reading and recording data. Direct current test conditions are supplied through digital control boxes and the output interference levels are monitored by a comparator box. The comparator box responds to device output voltage changes exceeding the test susceptibility threshold limits. Figure 2 shows the general DC test setup for the digital devices. A more detailed explanation of the test configuration may be obtained from the "Integrated Circuit Electromagnetic Susceptibility Investigation - Test and Measurement Systems" [2].

2.2 Digital Results - RF susceptibility testing was performed at four frequencies: 0.22, 0.91, 3.0, and 5.6 GHz. The data collected includes the susceptibility threshold level, RF power at all fixture ports, and DC parameter measurements before, during, and after RF stimulation. All data were taken with RF applied to the most susceptible port (as measured at 3.0 GHz). A sample of the data taken on one TTL device is given in table 2. A "zero" RF power run, a maximum RF power run, and two additional power levels were taken on every device. For more detailed information on CMOS and hybrid devices and their data, see references 1 and 3.

2.2.1 Most Susceptible Port Results - The most susceptible port and DC bias conditions are given in table 3, as determined from testing at 3.0 GHz. As indicated by table 3, the output in a logical low state was found to be more susceptible than any other port, for 8 out of 10 devices. The two exceptions are the 7479 where the $\overline{\text{set}}$ terminal proved most sensitive and the 2002 where input 5 was found to be most susceptible.

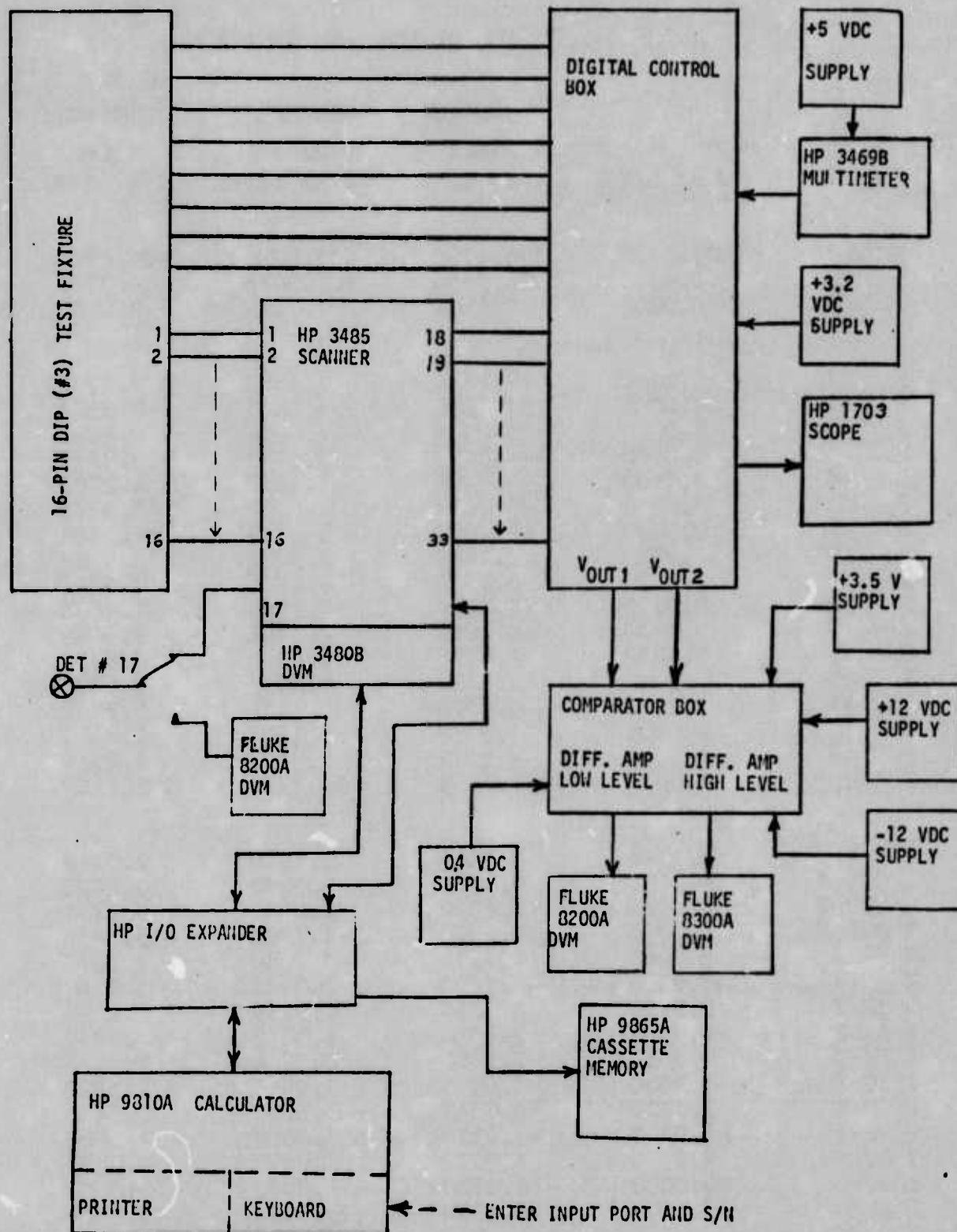


FIGURE 2 GENERAL TEST SETUP FOR DIGITAL DEVICE INTERFERENCE TESTING

Table 2 SUSCEPTIBILITY DATA FOR 7479 S.N. 309.022 AT 220 MHz

PARAMETER	0 RF LEVEL	MAXIMUM POWER		SUSCEPTIBILITY	
		1 RF LEVEL	2 RF LEVEL	THRESHOLD LEVEL	3 RF LEVEL
S.N.	309.0220	309.0220	309.0220	309.0220	
P DIS.	0.0000	1315.9654	102.8048	84.9767	
C.F.	0.0000	1.6894	1.7629	2.0795	
P 1	0.0000	17.7834	1.6582	1.2797	
P 2	0.0000	31.0838	1.0540	0.9381	
P 3	0.0000	91.0974	2.6254	2.1225	
P 4	0.0000	141.0455	28.5141	35.5444	
P 5	0.0000	91.7069	3.4535	3.2782	
P 6	0.0000	28.2884	1.2957	1.1271	
P 7	0.0000	59.4383	3.0793	1.5422	
P 8	0.0000	0.1419	0.0283	0.0247	
P 9	0.0000	0.0904	0.0243	0.0217	
P 10	0.0000	27.7834	1.7568	1.1595	
P 11	0.0000	44.4858	2.3358	1.3099	
P 12	0.0000	9.8965	0.6901	0.5454	
P 13	0.0000	10.6182	0.8796	0.6687	
P 14	0.0000	6.1778	0.4411	0.3747	
P 15	0.0000	16.5377	1.4323	1.0177	
P 16	0.0000	49.5649	2.2038	1.2356	
P INC.	0.0000	1941.7059	154.2772	137.1667	
V OUT 1	3.4940	0.1639	0.1246	2.0440	
I OUT 1	0.3800	0.0120	0.0090	0.2400	
V OUT 2	0.2064	3.5330	2.8620	0.2271	
I OUT 2	-15.5760	1.7600	-1.7700	-15.4690	
V IN 1	3.1980	3.1870	3.1990	3.1970	
I IN 1	-0.0100	-0.1400	-0.0200	-0.0200	
V IN 2	0.2218	0.7631	0.2219	0.2293	
I IN 2	0.9340	3.6480	0.9840	0.9230	
V IN 3	0.3852	1.5750	0.3244	0.3172	
I IN 3	1.7500	7.6910	1.4970	1.3600	
V IN 4	3.1980	3.0340	3.3890	3.3410	
I IN 4	-0.0100	-1.6700	1.8800	1.4200	
V CC	4.9550	4.9170	4.9430	4.9280	
I CC	-20.0000	-36.0000	-26.0000	-32.0000	
I GND	35.1100	35.6300	25.0000	45.7900	

Table 3 MOST SUSCEPTIBLE PORT AND DC BIAS CONDITIONS (3 GHz)

DEVICE NUMBER	RF ENTRY PORT/STATE	DC BIAS CONDITIONS AND (PIN NUMBERS)												
		INPUT (1)	INPUT (2)	OUTPUT (3)	V _{CC} (14)	GND (7)								
3021	OUTPUT/LOW	HIGH	HIGH	LOW	5.0 V	GND								
7432	OUTPUT/LOW	INPUT (1)	INPUT (2)	OUTPUT (3)	V _{CC} (14)	GND (7)								
		LOW	LOW	LOW	5.0 V	GND								
7402	OUTPUT/LOW	INPUT (2)	INPUT (3)	OUTPUT (1)	V _{CC} (14)	GND (7)								
		LOW	HIGH	LOW	5.0 V	GND								
7404	OUTPUT/LOW	INPUT (1)	OUTPUT (2)	V _{CC} (14)	GND (7)									
		HIGH	LOW	5.0 V	GND									
7405	OUTPUT/LOW	INPUT (1)	OUTPUT (2)	V _{CC} (14)	GND (7)									
		LOW	LOW	5.0 V	GND									
7450	OUTPUT/LOW	INPUT (9)	INPUT (10)	INPUT (13)	INPUT (1)	E (11)	F (12)	OUTPUT (8)	V _{CC} (14)	GND (7)				
		LOW	LOW	HIGH	HIGH	(OPEN)	(OPEN)	LOW	5.0 V	GND				
7473	OUTPUT Q/LOW	INPUT J (4)	INPUT K (3)	CLOCK (1)	RESET (1)	OUTPUT Q (12)	OUTPUT Q̄ (13)	V _{CC} (14)	GND (7)					
		HIGH	LOW	LOW	HIGH	HIGH	LOW	5.0 V	GND					
7479	SET/HIGH	INPUT D (2)	CLOCK (3)	SET (4)	RESET (1)	OUTPUT Q (5)	OUTPUT Q̄ (6)	V _{CC} (14)	GND (7)					
		LOW	LOW	HIGH	HIGH	HIGH	LOW	5.0 V	GND					
4011	OUTPUT/LOW	INPUT (1)	INPUT (2)	OUTPUT (3)	V _{DD} (14)	V _{SS} (7)								
		HIGH	HIGH	LOW	5 V	GND								
2002	INPUT 5/HIGH	INPUT 1 (1)	INPUT 2 (2)	INPUT 3 (3)	INPUT 4 (4)	INPUT 5 (9)	OUTPUT B (6)	OUTPUT C (8)	OUTPUT E (7)	V _{CC} (10)	5 V	GND		
		LOW	LOW	LOW	LOW	HIGH	(OPEN)	HIGH	GND					

2.2.2. Susceptibility Threshold Levels - The susceptibility threshold level data obtained at the most susceptible port may be represented in graphical form. Figure 3 shows the range of susceptibility levels (indicating the minimum and maximum RF power levels) and the average for all of the digital devices tested. This figure is a composite of data on 10 different device types, and thus shows a wide range of RF power required for susceptibility. A cross (X) at the average point indicates that not all devices tested reached the susceptibility threshold at the maximum power level applied. An arrow at the maximum indicates that at least one device did not reach the susceptibility threshold level indicated. The maximum power that may be injected into a device in interference testing is limited by the capability of the crystal detectors used to monitor power (each detector has a maximum power capability of 100 mW). Therefore, arrows indicate that the power required to reach the susceptibility threshold is greater than the maximum power which is shown by the arrows, and that the average is also greater than that indicated by the cross (X). At 0.22 GHz, susceptibility threshold limits were reached on 100% of the devices tested. Susceptibility threshold limits were reached on 98% at 0.91 GHz, 89% at 3.0 GHz, but only 29% at 5.6 GHz. The significance of the average, minimum, and maximum points is directly related to the percent indicated. Thus, at 5.6 GHz, the values indicated are probably far below actual susceptibility threshold levels. An increase in coupling through the ICs at 5.6 GHz reduces power dissipation in the test devices. That is, more power is coupled through the device and out other terminals and causes maximum detector limits to be reached at low internal power dissipation levels. In general, however, figure 3 indicates that susceptibility decreases with increasing frequency.

Individual graphs for each device are given in figures A-1 through A-10 (appendix A) in which an arrow at both maximum and minimum indicates that a susceptibility threshold was not reached on any of the test devices. The data used to construct

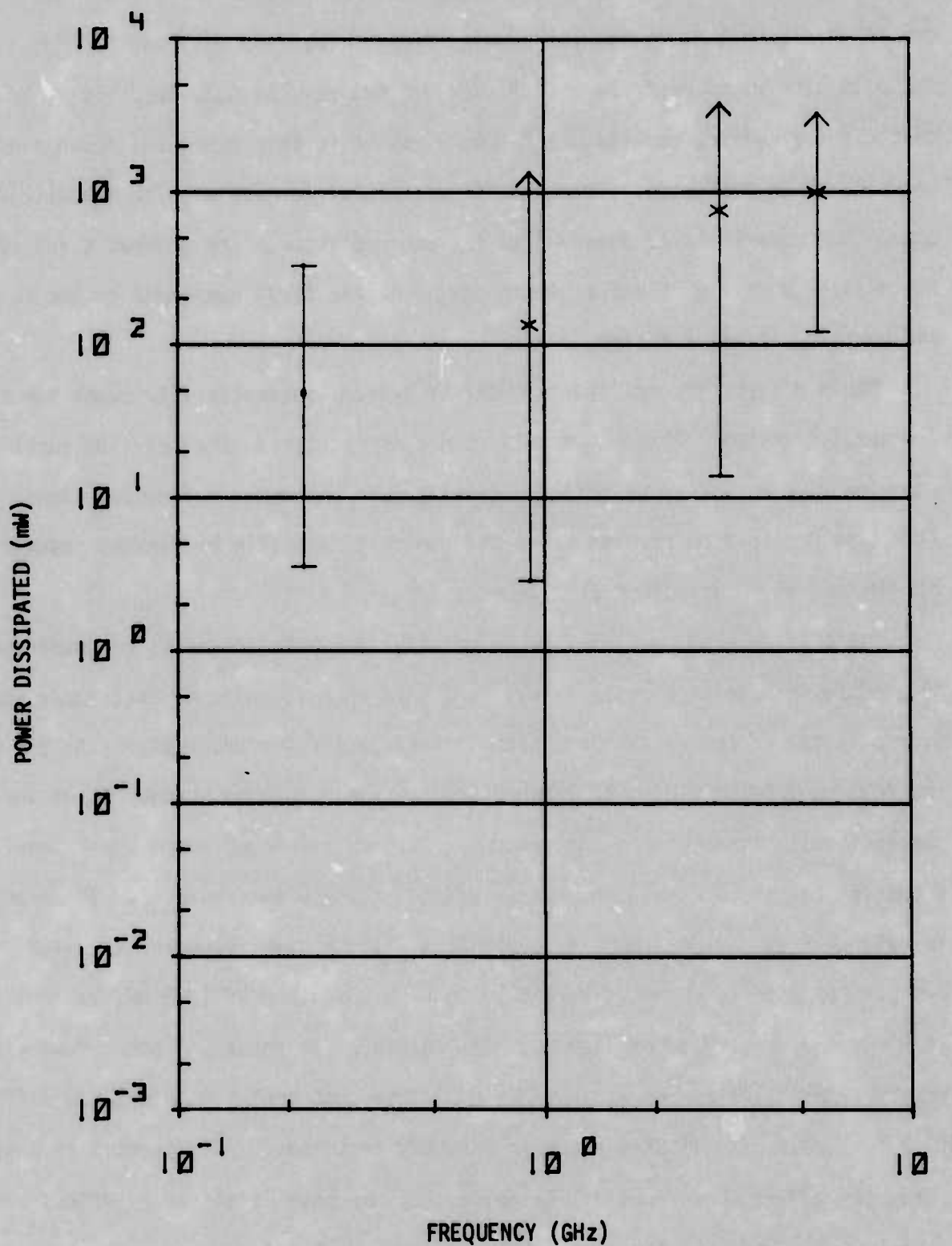


FIGURE 3 SUSCEPTIBILITY LEVEL RANGE FOR 10 DIGITAL DEVICES
(SAMPLE SIZE = 5 FOR EACH TYPE)

susceptibility graphs are contained in Appendix B. Graphs for all devices except the 7479 (figure A-8) follow the general trend. The 7479 dual type D flip-flop was found to be more susceptible at 0.91 and 3.0 GHz than at 0.22 GHz. It is possible that internal device coupling of RF could result in this type of a trend and this needs to be investigated. Coupling effects would increase with frequency and thus oppose the general trend observed in the other devices. The general trend may hold for devices when the RF has a direct effect on the first component on the IC chip and coupling is not a factor.

Table 4 lists the devices in order of average susceptibility level for the frequencies tested. Although some variance is indicated, the relative ranking of a device appears not to be affected greatly over the frequency range. Again the 7479 type D flip-flop perhaps shows the greatest exception by ranking seventh at 220 MHz and first at all other frequencies.

Table 4 is based upon average values (for a sample lot of 5) of power required to produce interference while figures A-1 through A-10 indicate that there can be over a factor of ten spread in susceptibility levels for one device. At 220 MHz, the 7432 quad 2-input OR gate (figure A-2) is shown to have a power level for susceptibility threshold on one device at 12.6 mW (minimum) and a power level for a susceptibility threshold on another device at 331.6 mW (maximum). The average for all devices is 104.2 mW. In comparison, at the same frequency the 7402 quad 2-input NOR gate is shown (figure A-3) to have a minimum of 13.2 mW, maximum of 15.5 mW, and an average of 14.9 mW. The variance for these and other devices can result from: 1) differences in individual chip component parameters, 2) differences in chip layout, and 3) difference in assembly techniques. Differences in these areas can affect RF susceptibility while they may have little or no effect on the normal device specifications.

Table 4 SUSCEPTIBILITY LEVELS FOR DIGITAL DEVICES

0.22 GHz	
DEVICE NUMBER	AVE. SUSCEPTIBILITY THRESHOLD LEVEL (mW)
7450	6.5
7404	7.5
7473	9.9
7402	14.9
3021	25.3
4011	27.7
7405	29.4
7479	81.2
7432	104.2
2002	194.0

0.91 GHz	
DEVICE NUMBER	AVE. SUSCEPTIBILITY THRESHOLD LEVEL (mW)
7479	9.1
7404	22.9
7450	28.6
7402	42.3
7473	70.8
7405	127.7
3021	149.4
4011	220.0
Δ 7432	> 336.6
2002	470.0

3.0 GHz	
DEVICE NUMBER	AVE. SUSCEPTIBILITY THRESHOLD LEVEL (mW)
7479	26.3
7402	87.0
7450	106.8
7404	192.1
7473	735.0
2002	780.0
4011	935.0
Δ 7405	> 1125.6
3021	1581.6
Δ 7432	> 2259.6

5.6 GHz	
DEVICE NUMBER	AVE SUSCEPTIBILITY THRESHOLD LEVEL (mW)
7479	166.7
7404	420.6
* 4011	> 486.4
Δ 7450	> 692.8
* 2002	> 750.0
* 3021	> 1017.5
* 7402	> 1051.7
* 7432	> 1359.1
* 7405	> 1741.7
* 7473	> 2303.1

Δ SUSCEPTIBILITY THRESHOLD LEVELS NOT REACHED ON ALL DEVICES

* SUSCEPTIBILITY THRESHOLD LEVELS NOT REACHED ON ANY DEVICE

2.2.3 Multiple Susceptibility Threshold Levels - In addition to determining the minimum power level at which a susceptibility threshold level is reached, it was also observed that at higher power levels or for long duration RF pulses, additional or multiple thresholds were reached. (These phenomena were observed and are presented here but it was beyond the scope of this survey to pursue them further.) Multiple susceptibility threshold levels have been observed on two devices.

Devices from the 7473 J-K flip-flop test group exhibited both high and low level susceptibility thresholds. With 7473 devices biased as indicated in table 3, application of 500 μ sec, 220 MHz RF pulses to the \bar{Q} terminal was found to cause output Q(high) to vary with increasing RF power and RF pulse duration. The scope traces of figure 4 exhibit increasing RF power level in the order labeled 1 through 5. Output Q is shown to increase above 5.0 V resulting in a high limit threshold being reached (see trace 2 of photo in figure 4). Increasing power would then result in both high and low level thresholds being reached as demonstrated by trace 4. Further increases in power result in a single low-level threshold being reached as indicated

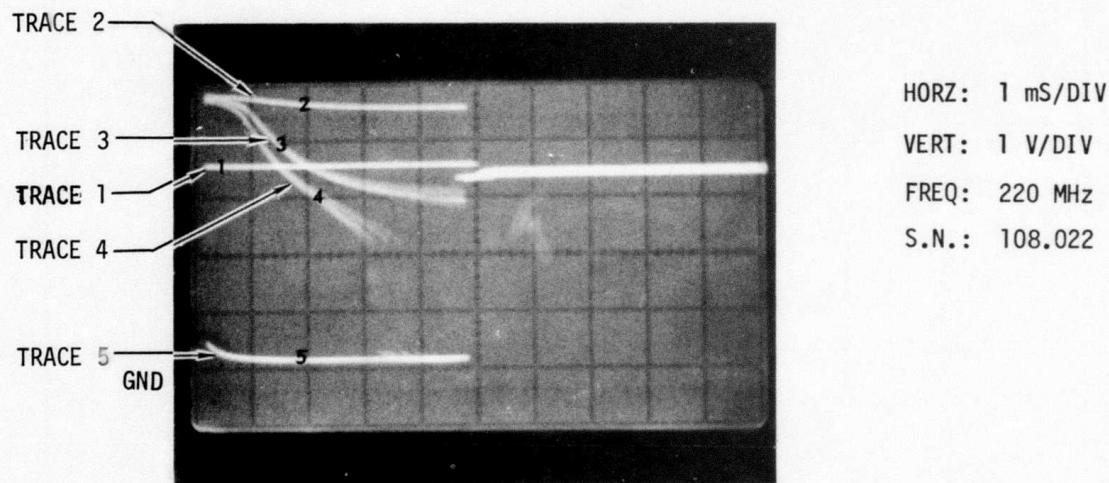


FIGURE 4 MULTIPLE SUSCEPTIBILITY THRESHOLD LEVELS OF THE 7473 DUAL J-K FLIP-FLOP, OUTPUT Q

by trace 5. As shown by the photo, the device recovered from the low level of trace 5 at the end of the 500 μ sec RF pulse indicating that the output did not toggle states. These data display a large interference mode dependence upon RF power level.

The 7479 type D flip-flop, on the other hand, exhibited no multiple susceptibility thresholds but did toggle output states at all frequencies. Figure 5 shows the average, minimum, and maximum power required to force the 7479 to toggle. Comparing to figure A-8, (7479 susceptibility levels), the RF power levels required to produce output toggle were not far from levels required to just reach a susceptibility threshold. Figure 5 exhibits the same anomaly of the device being more sensitive at 0.91 and 3.0 GHz than at 0.22 GHz.

As shown in figure 6, the 7432 quad 2-input OR gate biased as indicated in table 3, demonstrated both high level (point A) and low level (point B) susceptibility thresholds. The photo shows 220 MHz CW RF power turning on at point A and remaining on past point B. This device exhibits a susceptibility level dependence upon duration of applied RF. This time-dependence appears to be related to heating of the IC chip. That is, heat and RF effects simultaneously cause chip parameter changes affecting the output voltage.

2.2.4 Susceptibility Threshold Level Dependence Upon RF Duration - Observation of device behavior indicates interference level changes (although sometimes slight) with time for CW RF power. The 7432 OR gate exhibits this characteristic. Both increases and decreases in RF effects are observed. In general, the RF-produced interference effects are observed to increase with time at 220 MHz. While at 0.91, 3.0, and 5.6 GHz, the effects decrease with time. The basis for this dependence may be related to heating caused by the RF power. Changes in heating effects could be related to coupling changes that would be frequency dependent. That is, the paths taken by RF through the device via coupling could vary with frequency, thus RF stimulation and heating could occur in different areas as frequency changes.

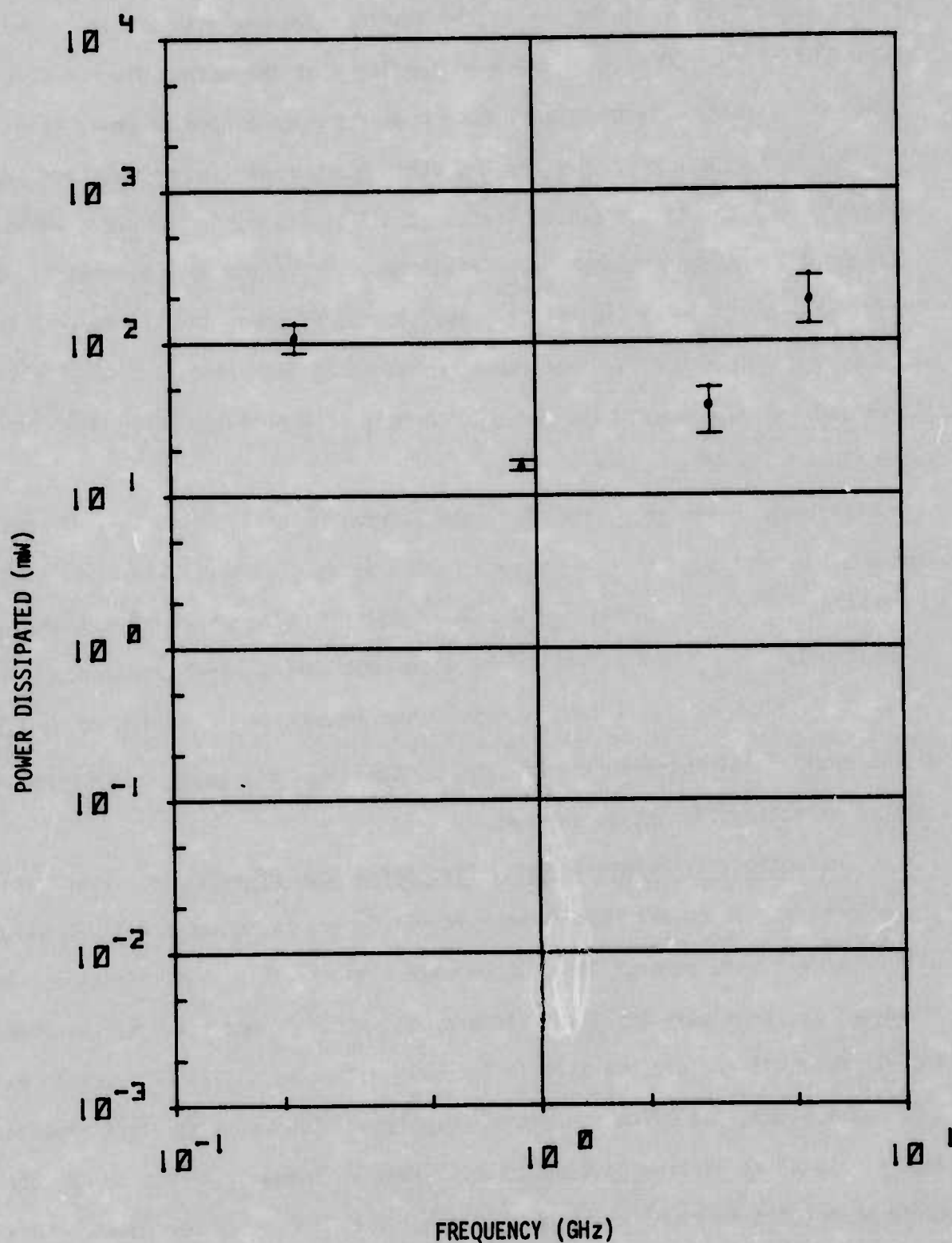


FIGURE 5 AVERAGE OUTPUT TOGGLE LEVEL FOR 7479
(SAMPLE SIZE = 5)

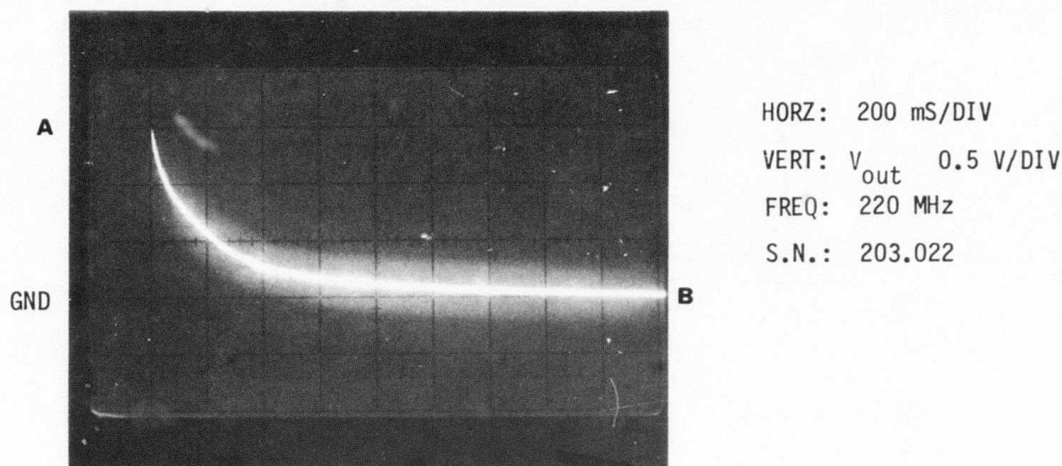


FIGURE 6 TIME RELATED MULTIPLE SUSCEPTIBILITY THRESHOLD LEVELS
OF THE QUAD 2-INPUT OR GATE

Further investigation is required before any definite conclusions may be made in this area.

2.2.5 Data Correlations - The digital devices tested (see table 1) were chosen in an attempt to cover the more common logic functions available in the TTL family plus a small sampling of MOS and hybrid devices. The devices which rank in the upper 40% for a most susceptible criterion are shown in table 5. As indicated, the 7404, 7450, 7402, and 7479 (all TTL devices) appear most frequently. The most sensitive port on the 7402, 7404, and 7450 was found to be the output in a logical low state. The most sensitive port on the 7479 was the \overline{set} in a logical high state. The circuit diagrams of all devices are contained in Appendix E.

Comparing circuits reveals that all of the TTL low state output circuits are represented identically. The TTL high state output circuits differ in a resistance value of 100 to 130 ohms except for the 7405 which is an open collector output. Because of similarity of device outputs, it would appear that variance in component (or parasitic) parameters may be responsible for the different susceptibility

TABLE 5 DEVICES EXHIBITING HIGH SUSCEPTIBILITY

DEVICE NUMBER	NUMBER OF TIMES APPEARING IN UPPER 40% OF MOST SUSCEPTIBLE DEVICES	DEVICE TYPE	DEVICE LOGIC FUNCTION
7404	4	TTL	HEX INVERTER
7450	4	TTL	EXPANDABLE DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE
7402	3	TTL	QUAD 2-INPUT NOR GATE
7479	3	TTL	QUAD TYPE D FLIP-FLOP
7473	1	TTL	DUAL TYPE J-K FLIP-FLOP
4011	1	CMOS	QUAD 2-INPUT NAND GATE

threshold levels among devices. Another possibility is that the remainder of the circuitry, although not directly subjected, is causing the output to malfunction (indirect effect).

Coupling and effects on parasitic elements may be involved. Some interference effects can be explained by RF rectification at pn junctions (both parasitic junctions and functional circuit junctions). The "Bipolar NAND Gate Study" [4] gives a detailed approach to analyzing RF effects on the 7400 NAND gate based on junction rectification. The 7400 is a TTL device in the same family; thus, results should be applicable to the effects on these devices.

In order to compare RF susceptibility levels of standard, low power, and high speed TTL devices, the 7404, 74L04, and 74H04 hex inverters were tested for RF interference at 220 MHz. Results are depicted in figure 7. Of the samples tested, the 7404 is the most susceptible, the 74L04 next, and the 74H04 least. However, as shown, the 74L04 has a wide spread from minimum to maximum. Its spread completely covers the 7404 range and a portion of the 74H04.

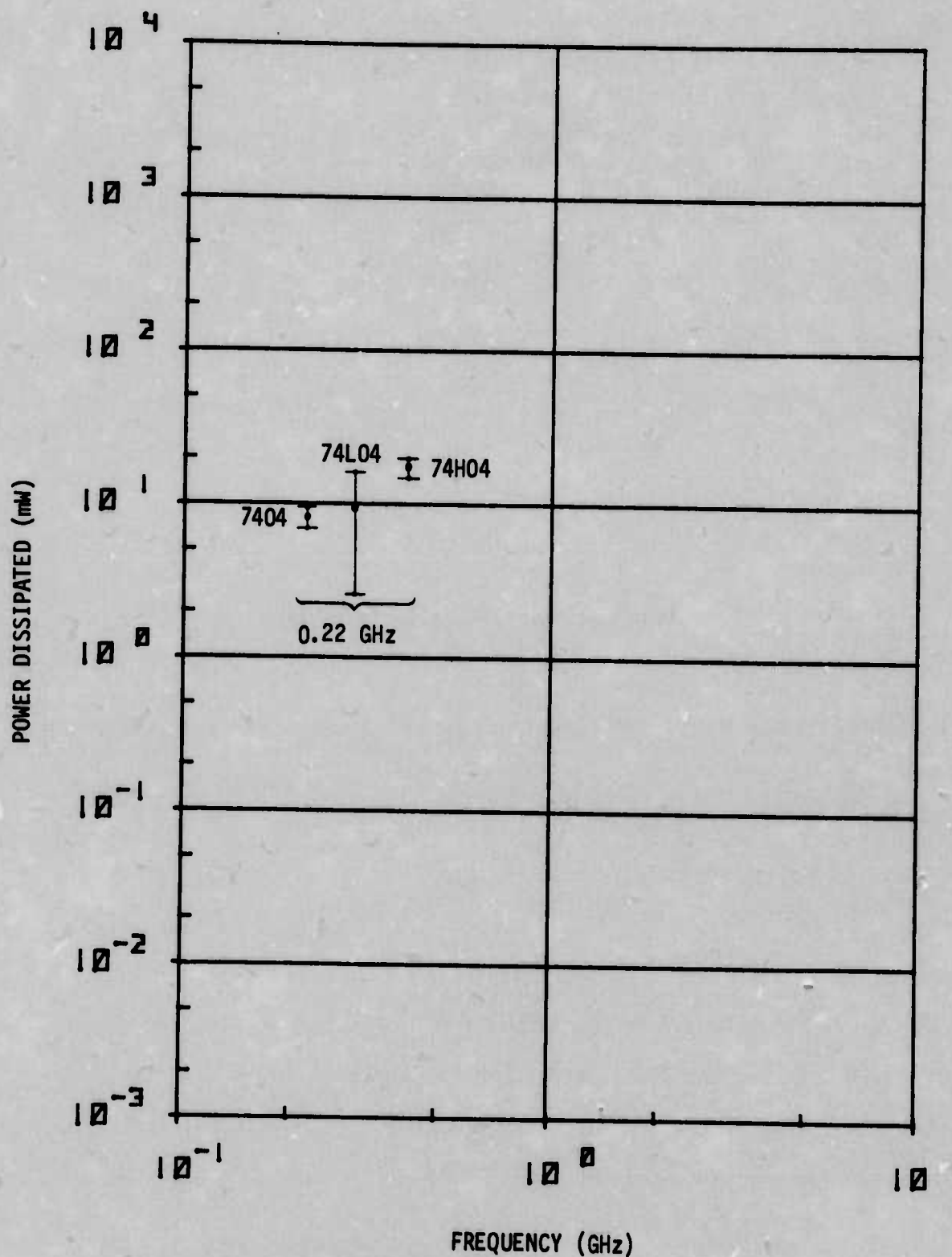


FIGURE 7 COMPARISON OF 7404, 74L04, AND 74H04 RF SUSCEPTIBILITY LEVELS
(SAMPLE SIZE = 5)

INTEGRATED CIRCUIT SUSCEPTIBILITY

MDC E1126
9 AUGUST 1974

3. LINEAR DEVICE SAMPLE

The 10 linear devices chosen for RF testing are given in table 6. The types of devices chosen are commonly utilized in circuit design.

3.1 Linear Test Plan - All testing was performed at 0.22, 0.91, 3.0, and 5.6 GHz with devices operating under normal DC bias conditions. As with the digital devices, the most sensitive port was determined at 3.0 GHz by injecting RF into each port while monitoring the DC parameters. Testing at all frequencies was then performed at the most susceptible port determined at 3.0 GHz.

Direct current parameter and RF power values at all fixture ports were measured before, during, and after RF stimulation. These measurements were made and recorded with zero RF power applied, with RF power applied at a minimum level to reach a susceptibility threshold, and at two additional levels. Five devices of each type were used for the test sample. The susceptibility threshold level is discussed in paragraph 3.1.3.

3.1.1 Susceptibility Threshold Limits - Levels of interference can not be as well defined for linear devices as they are for digital. This is because the changes in parameters (which would be considered to interfere with the operation of a circuit using a linear device) depend much more on actual design constraints. That is, the accuracy or stability with which a voltage or current must be maintained by a device depends upon the particular circuit requirement. Digital devices generally are required merely to interface with each other under manufacturer-specified rules. A ± 0.5 volt change in the output voltage level was chosen as the susceptibility threshold limit for the operational amplifier, the voltage regulator, and for the input differential which must be overcome at the input of the comparator. This level is chosen for test purposes and is not intended to indicate that changes of less than ± 0.5 volt would not be significant in some applications.

Table 6 LINEAR DEVICE SAMPLE

DEVICE NUMBER	DEVICE TYPE
201	OPERATIONAL AMPLIFIER
307	OPERATIONAL AMPLIFIER
310	VOLTAGE FOLLOWER
316	OPERATIONAL AMPLIFIER
324	QUAD OPERATIONAL AMPLIFIER
339	QUAD COMPARATOR
725	INSTRUMENTATION OPERATIONAL AMPLIFIER
747	DUAL OPERATIONAL AMPLIFIER
309	POSITIVE VOLTAGE REGULATOR
320	NEGATIVE VOLTAGE REGULATOR

3.1.2 Test Setup - Testing was controlled by an HP 9810A programmable calculator using a 50-channel scanning DVM and cassette memory for reading and recording data. RF power, DC voltage, and DC current were measured and recorded at every device port. Changes in output voltage (refer to 3.1.1) were used as an indication of device interference. Direct current test conditions were supplied through the operational amplifier, comparator, and voltage regulator control boxes. These boxes bias devices to normal operating conditions. Output susceptibility levels were monitored by the comparator box which responded to device output voltage changes in excess of the susceptibility threshold limits. Schematics of the test boxes are contained in the "Test and Measurement Systems" report [2].

Figures 8 through 17 show the DC test configurations and RF input for each of the devices. All operational amplifiers were connected as inverters with a gain of 10 (OUTPUT VOLTAGE = -10 (INPUT VOLTAGE)). The input voltage supplied was +0.5 volt resulting in a normal output voltage of -5.0 volts. The voltage regulators are fixed output types of +5.0 volts (309) and -5.0 volts (320). The 309 received a +6.0 volt input and the 320 a -7.0 volt input.

The comparator (330) was biased with a 0.5 volt differential at the inputs. The inverting input at 4.5 volts and the non-inverting input at 5.0 volts result in an output voltage of approximately 0.1 volt. The output behaves similar to a digital device in that it has two stable states, 0.1 volt and 5.0 volts relative to the comparison made at the inputs. With the non-inverting input more positive, the output is at 5.0 volts, and with the inverting input more positive, the output is at 0.1 volt. The output interference levels were chosen to be $0 \text{ volts} < V_{\text{out}} < 1.0 \text{ volt}$ for the comparator in the nominal 0.1 volt output state as biased in the DC test circuit.

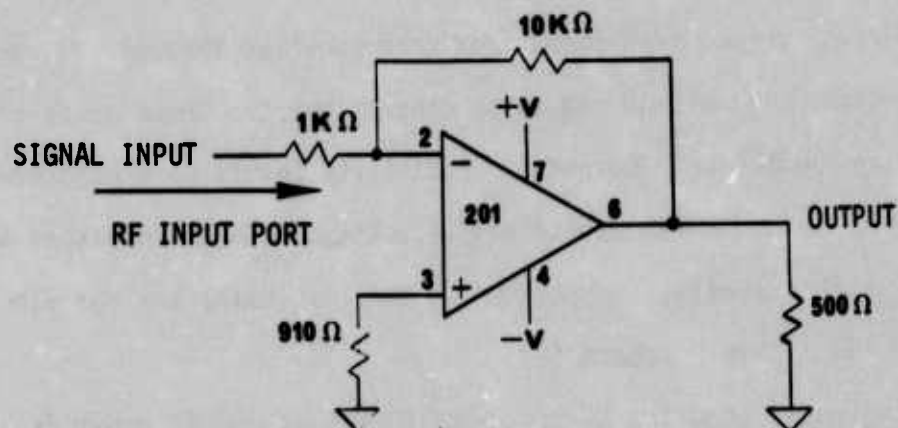


FIGURE 8 201 DC TEST CIRCUIT

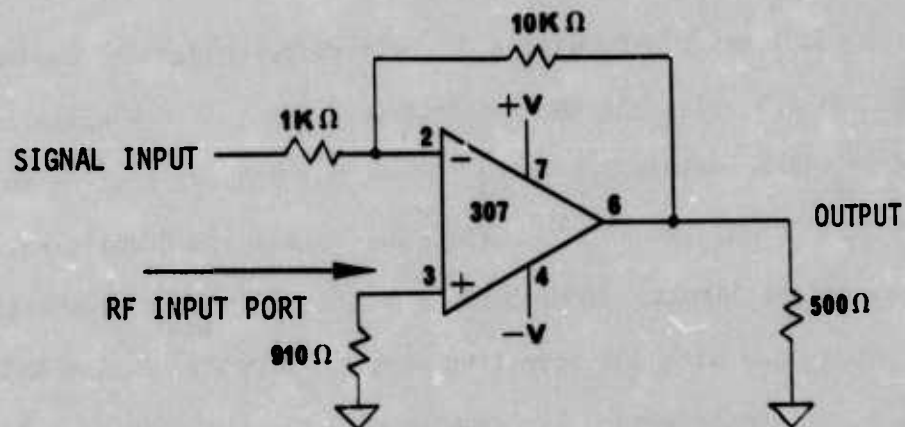


FIGURE 9 307 DC TEST CIRCUIT

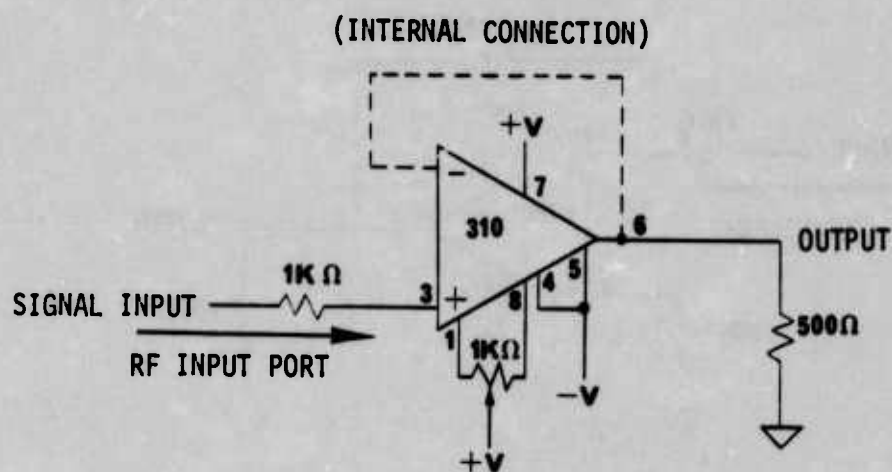


FIGURE 10 310 DC TEST CIRCUIT

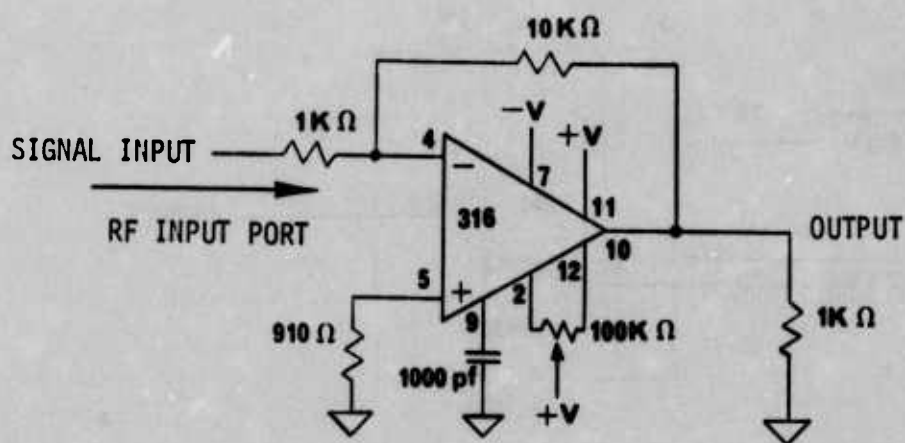


FIGURE 11 316 DC TEST CIRCUIT

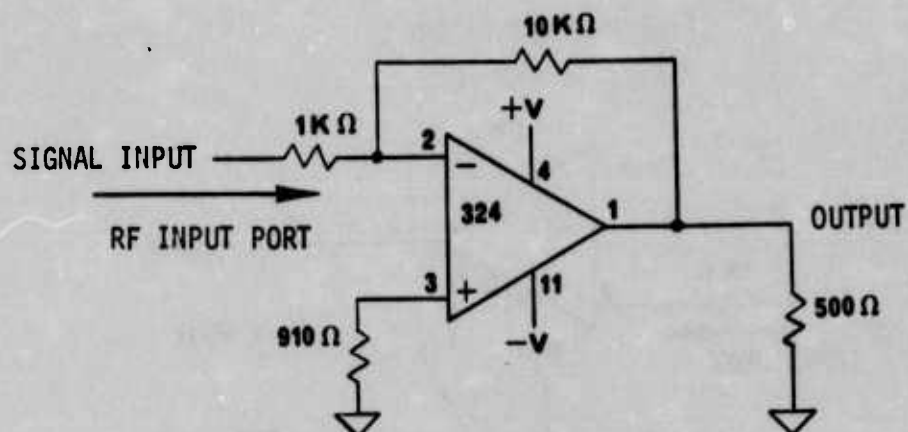


FIGURE 12 324 DC TEST CIRCUIT

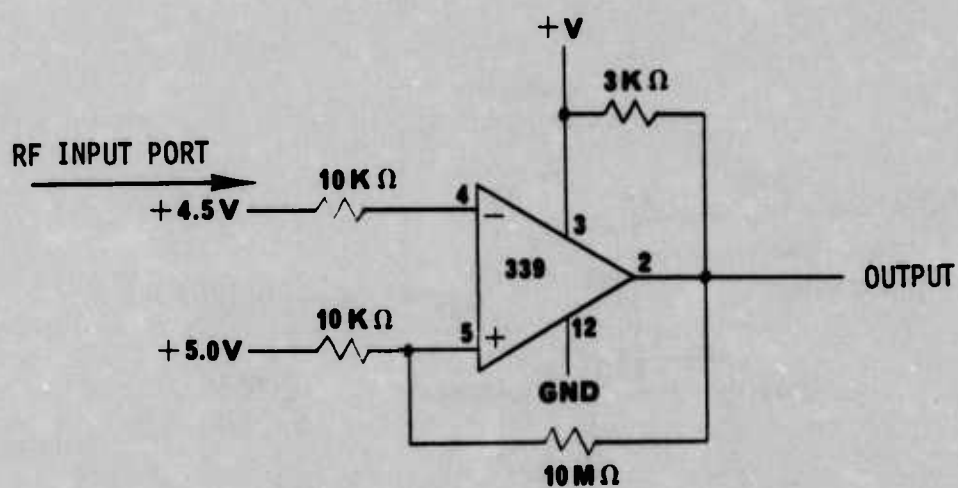


FIGURE 13 339 DC TEST CIRCUIT

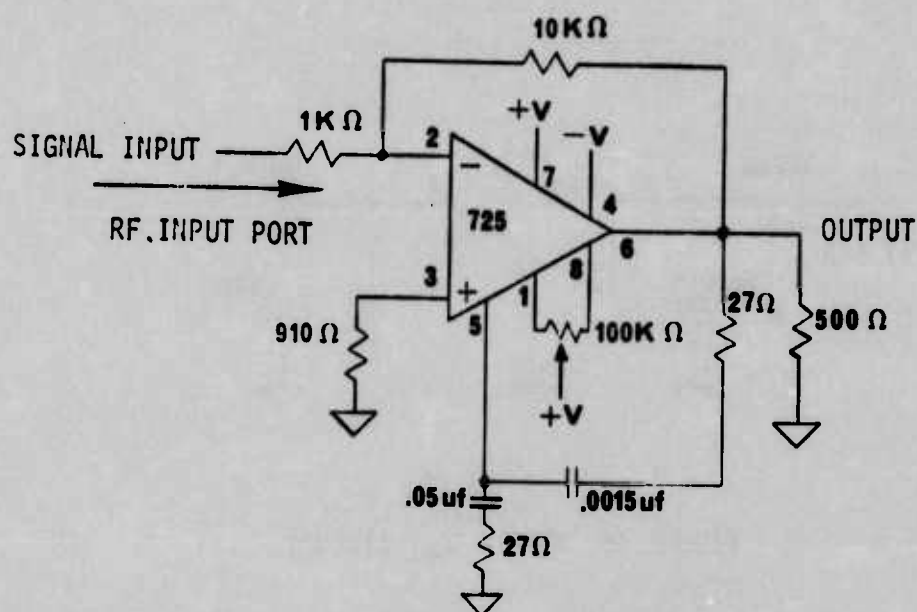


FIGURE 14 725 DC TEST CIRCUIT

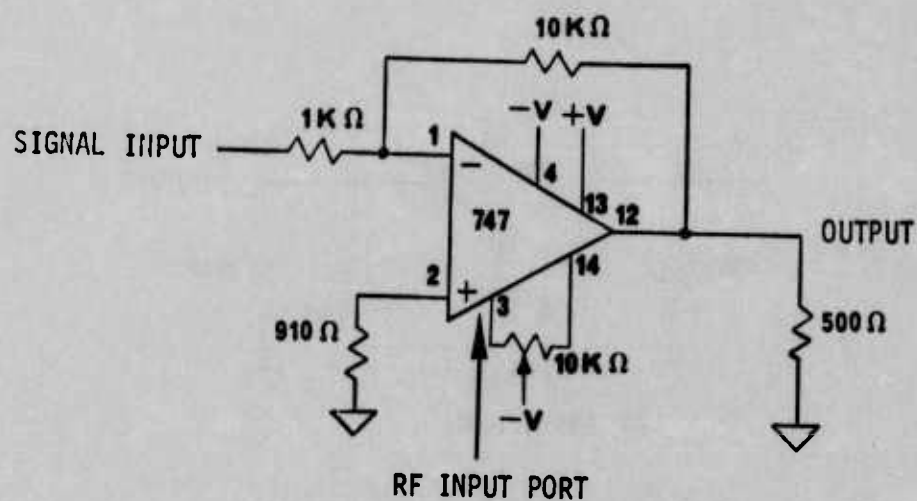


FIGURE 15 747 DC TEST CIRCUIT

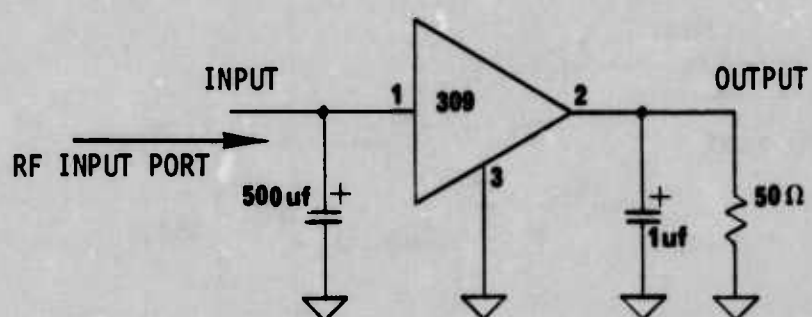


FIGURE 16 309 DC TEST CIRCUIT

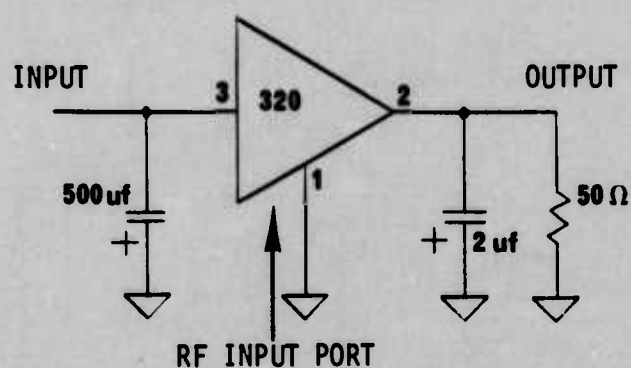


FIGURE 17 320 DC TEST CIRCUIT

3.2 Linear Results - RF susceptibility testing was performed at 0.22, 0.91, 3.0 and 5.6 GHz on the most susceptible ports determined at 3.0 GHz. The data collected include susceptibility level determination and DC parameter measurements, before, during, and after RF stimulation.

3.2.1 Most Susceptible Port Results - Table 7 shows the most susceptible port and DC bias conditions. In general, a device input (usually the inverting input) is shown to be most susceptible in the configurations tested. The 747 operational amplifier and 320 negative voltage regulator were the exceptions.

3.2.2 Susceptibility Threshold Levels - Susceptibility level data is represented in figure 18 as a composite of the 10 linear devices tested. Figures C-1 through C-10 (contained in Appendix C) are plots of the susceptibility level data for each linear device tested. The linear susceptibility level data used to construct the graphs are contained in Appendix D. As shown in Appendix D, the devices tested exhibit a wide range in power required to reach a susceptibility threshold level. The general trend is a decrease in susceptibility with increasing frequency except that the susceptibility threshold levels at 0.91 GHz are usually above those at 3.0 GHz and sometimes above those at 5.6 GHz. Figures C-1 through C-10 show that the 339 (figure C-6) and 725 (figure C-7) are the only two devices for which the 0.91 GHz level is lower than the 3.0 GHz level. For the 747 (figure C-8) and the 309 (figure C-9), the interference at 0.91 GHz is shown to be higher than at all other frequencies tested. As indicated by figure C-9, a susceptibility level for the 309 was not reached at any of the four frequencies tested. Also figure C-7 indicates that a susceptibility level was not reached at 5.6 GHz for the 725. Thus the susceptibility threshold limits were reached by 90% of the devices at 0.22 GHz, 0.91 GHz, and 3.0 GHz, and 80% at 5.6 GHz.

In figures C-1 and C-8 the dashed arrows indicate the possibility of a lower susceptibility level. As previously mentioned, all susceptibility threshold levels were determined by a 500 μ sec RF pulse which was calibrated with a CW power

Table 7 MOST SUSCEPTIBLE PORT AND DC BIAS CONDITIONS (3 GHz)

DEVICE NUMBER	RF ENTRY PORT	DC BIAS CONDITIONS AND (PIN NUMBERS)									
		INVERTING INPUT (2)	NON-INVERTING INPUT (3)	OUTPUT (6)	+V (7)	-V (14)					
201	INVERTING INPUT	+0.5 V	GND	-5.0 V	+12.0 V	-12.0 V					
307	NON-INVERTING INPUT	INVERTING INPUT (2)	NON-INVERTING INPUT (3)	OUTPUT (6)	+V (7)	-V (14)					
		+0.5 V	GND	-5.0 V	+12.0 V	-12.0 V					
310	NON INVERTING INPUT	NON-INVERTING INPUT (3)	OUTPUT (6)	BALANCE (1)	BALANCE (8)	BOOSTER (5)	+V (7)	-V (4)			
		-5.0 V		EACH END OF 1K POT, WIPER TO +V		CONNECTED TO PIN 4	+12 V	-12 V			
316	INVERTING INPUT	INVERTING INPUT (4)	NON-INVERTING INPUT (5)	BALANCE (2)	BALANCE (12)	OUTPUT (10)	COMPENSATION (9)	+V (11)	-V (7)	GUARD (6)	
		+0.5 V	GND	EACH END OF 100K POT, WIPER TO +V		-5.0 V	1000 pf	+12 V	-12 V	(OPEN)	
324	INVERTING INPUT	INVERTING INPUT (2)	NON-INVERTING INPUT (3)	OUTPUT (1)	+V (4)	-V (11)					
		+0.5 V	GND	-5.0 V	+12 V	-12 V					
339	INVERTING INPUT	INVERTING INPUT (4)	NON-INVERTING INPUT (5)	OUTPUT (2)	+V (3)	-V (12)					
		+0.5 V	GND	-5.0 V	+12 V	-12 V					
725	INVERTING INPUT	INVERTING INPUT (2)	NON-INVERTING INPUT (3)	OUTPUT (6)	OFFSET NULL (1)	OFFSET NULL (8)	FREQUENCY (5) COMPENSATION	+V (7)	-V (4)		
		+0.5 V	GND	-5.0 V	EACH END OF 100K POT, WIPER TO +V	SEE FIGURE 34		+12 V	-12 V		
747	OFFSET NULL (3)	INVERTING INPUT (1)	NON-INVERTING INPUT (2)	OUTPUT (2)	OFFSET NULL (3)	OFFSET NULL (14)	+V (13)	-V (4)			
		+0.5 V	GND	5.0 V	EACH END OF 10 K POT, WIPER TO -V		+12 V	-12 V			
309	INPUT	INPUT (1)	OUTPUT (2)	GND (3)							
		6 V	5 V	GND							
320	GND	INPUT (3)	OUTPUT (3)	GND (1)							
		-7 V	-5 V	GND							

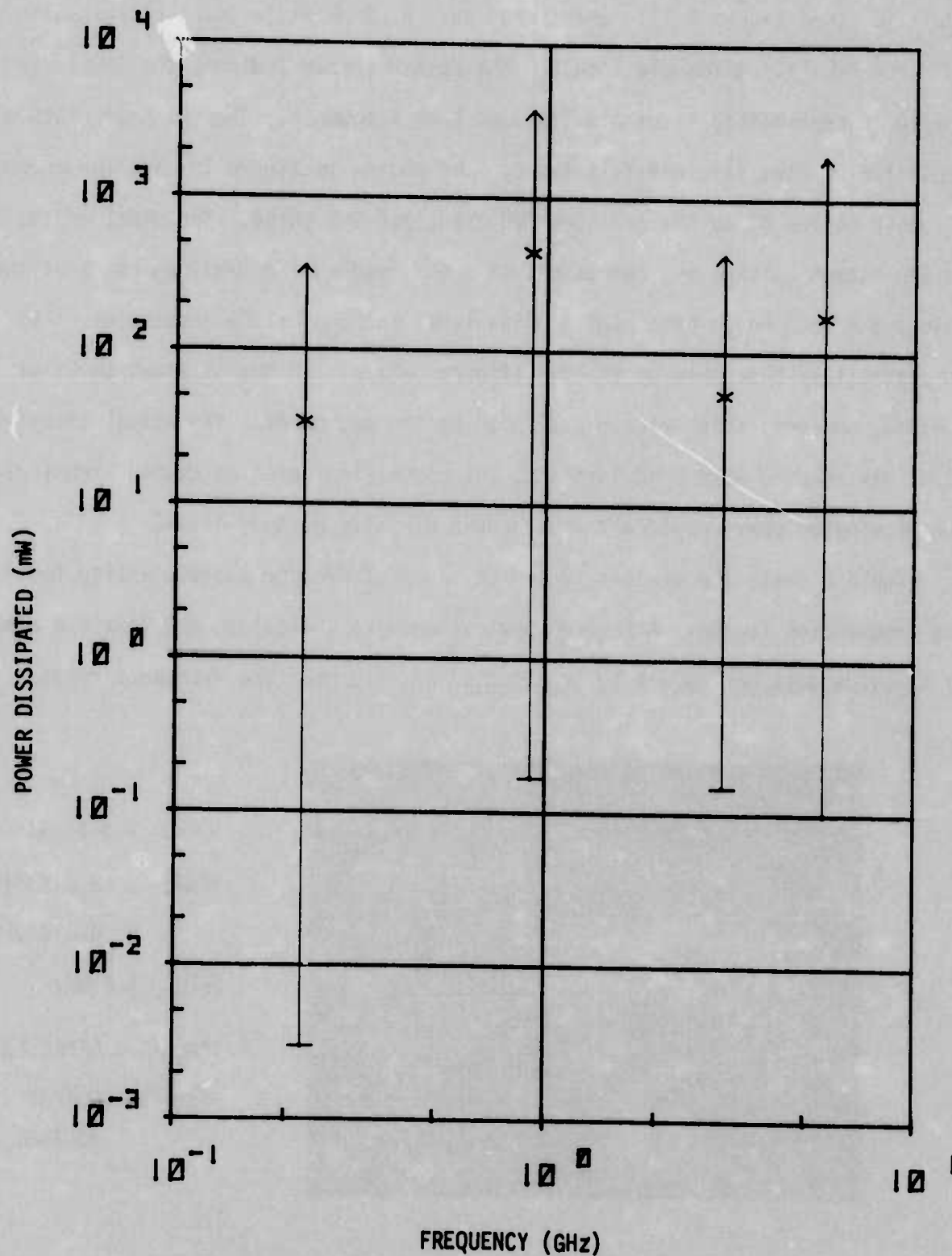


FIGURE 18 SUSCEPTIBILITY LEVEL RANGE FOR 10 LINEAR DEVICES
(SAMPLE SIZE = 5 FOR EACH TYPE)

measurement. This was done to minimize heating problems. However, the 201 operational amplifier (see figure C-1) demonstrated over a 10 dB difference between pulsed and CW susceptibility threshold levels. The dashed arrows indicate the level for a pulsed susceptibility threshold limit at each frequency. The 201 appears to also be sensitive to fast rise and fall times. The photos in figure 19 show the output response (trace B) to the detected 500 μ sec, 5.6 GHz pulse. The peaks of the ringing on the output voltage are coincident with the leading and trailing edges of the detected RF and reach both high and low level susceptibility thresholds. The susceptibility threshold of the 747 (figure C-8) at 220 MHz is shown to be at 0.01 mW, however, this value was limited by the equipment. The actual interference level was reached with 5 dB less incident power (indicated by dashed arrow) although the dissipated power could not be measured directly at this level.

Table 8 lists the devices tested in order of average susceptibility level for the frequencies tested. Although some variance is indicated, the relative ranking of a device does not appear to be affected greatly over the frequency range.

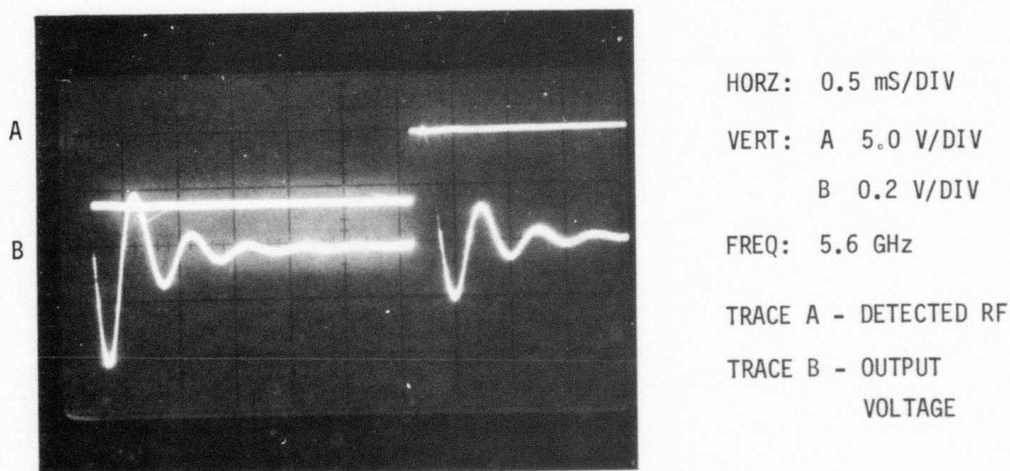


FIGURE 19 PULSE INTERFERENCE RESPONSE OF 201

TABLE 8 AVERAGE SUSCEPTIBILITY LEVELS FOR LINEAR DEVICES

0.22 GHz	
DEVICE NUMBER	AVE. SUSCEPTIBILITY THRESHOLD LEVEL (mW)
324	.007
747	.01
307	.027
201	.42
310	.545
316	.745
320	2.05
725	2.88
339	10.24
* 309	> 327.6

0.91 GHz	
DEVICE NUMBER	AVE. SUSCEPTIBILITY THRESHOLD LEVEL (mW)
324	1.34
747	2.56
316	2.67
307	3.08
201	3.81
339	19.7
725	41.2
310	43.8
320	754.6
* 309	> 3532.2

3.0 GHz	
DEVICE NUMBER	AVE. SUSCEPTIBILITY THRESHOLD LEVEL (mW)
747	.23
324	.542
307	.694
201	1.67
316	2.58
339	6.25
310	23.4
320	46.6
725	213.1
* 309	>238.4

5.6 GHz	
DEVICE NUMBER	AVE. SUSCEPTIBILITY THRESHOLD LEVEL (mW)
747	1.96
316	3.38
307	4.99
201	9.58
320	16.1
324	53.1
339	80.4
* 725	> 186.3
310	188.8
* 309	> 1196.0

* SUSCEPTIBILITY THRESHOLD LEVELS NOT REACHED ON ANY DEVICE

3.2.3 Multiple Susceptibility Levels - Multiple susceptibility levels were observed on only one device, the 201 operational amplifier. As previously discussed, the failures were observed to take place at turn-on and turn-off of the RF pulse. CW power applied to the device results in the output voltage reaching only a single low-level susceptibility threshold at a power level usually well above the level found with the pulse. Additional investigations of this type of effect are essential. Capacitive coupling on the chip may be involved in this type reaction.

3.2.4 Susceptibility Threshold Level Dependence Upon RF Duration - Little time dependence was observed on the linear devices tested. Low power levels were required to reach susceptibility threshold levels which would indicate less internal power dissipation and, thus, perhaps fewer internal heating problems. It may be a characteristic of the linear devices to be influenced less by internal RF heating.

3.2.5 Data Correlations - The linear devices chosen for testing include six operational amplifiers, two voltage regulators, one voltage follower, and one comparator (see table 6). The devices which rank in the upper 40% for a "most susceptible" criterion are shown in table 9.

Table 9 contains only operational amplifiers. The 307, 324, and 201 do not have external frequency compensation or balance adjust (offset null). The 747 has external balance adjust and the 316 has both external balance adjust and frequency compensation. The 309 (+5V) regulator was found to be the least susceptible of the linear devices tested, having never exceeded susceptibility threshold limits at any frequency. The 320 (-5V) regulator did not prove unsusceptible; instead, it exceeded susceptibility threshold limits at all frequencies and even ranked 5th at 5.6 GHz.

For the devices listed in table 9, the inverting input was found most susceptible on the 324, 201, and 316. The non-inverting input on the 307 and the offset null on the 747 were found to be most susceptible. Although the inverting input is usually the most susceptible port, the non-inverting input and offset null

Table 9 DEVICES EXHIBITING HIGH SUSCEPTIBILITY

DEVICE NUMBER	NUMBER OF TIMES APPEARING IN UPPER 40% OF MOST SUSCEPTIBLE DEVICES	DEVICE TYPE
747	4	DUAL OPERATIONAL AMPLIFIER
307	4	OPERATIONAL AMPLIFIER
324	3	QUAD OPERATIONAL AMPLIFIER
201	3	OPERATIONAL AMPLIFIER
316	2	OPERATIONAL AMPLIFIER

ports were the most susceptible on two devices. At the circuit diagram level, no indication of relative susceptibility is found. In-depth analysis and additional testing on DC parameters and specific RF tests are required before the RF effects can be effectively related to actual chip components including the parasitics. This type of approach is taken in the "Bipolar Op Amp" report [4].

INTEGRATED CIRCUIT SUSCEPTIBILITY

MDC E1126
9 AUGUST 1974

4. COMPARISON OF DIGITAL AND LINEAR TEST RESULTS

Comparison of digital and linear test results provide some basic information. As may be observed from tables 4 and 8, the linear devices generally prove more susceptible than the digital ones (at the frequencies shown.) At 220 MHz, the average interference level of the most susceptible linear device (324) is 29.6 dB below the most susceptible digital device (7450). At 0.91 GHz, the 324 is 8.3 dB below the 7479; at 3.0 GHz, the 747 is 20.6 dB below the 7479; and at 5.6 GHz, the 747 is 19.3 dB below the 7479. These are average values and, therefore, may not indicate the worst cases observed. In figure 20, the maximum and minimum susceptibility threshold levels observed are plotted. As shown, the minimum interference levels of the linear are below the digital at all frequencies tested, by these amounts: 30.8 dB at 220 MHz, 12.3 dB at 0.91 GHz, 19.7 dB at 3.0 GHz, and 31.0 dB at 5.6 GHz.

For the devices tested, the linear devices exhibit interference at RF power levels as much as 31.0 dB below digital devices. The maximum interference levels are shown, but they are not considered to be of interest to the design engineer. The designer is usually concerned with worst case conditions or minimum RF power levels at which circuit interference would take place.

For both linear and digital devices, the susceptibility threshold level generally increased with increasing frequency; with the data at 0.91 GHz being the exceptions. However, at 0.91 GHz, the level was found to be lower than the trend would indicate for the digital devices and higher for the linear devices. These effects at 0.91 GHz may be related to the device's basic fabrication techniques involving geometry of chip layout which could cause resonance at 0.91 GHz.

For digital devices, the most susceptible port was generally the output in the low state, while for the linear it was found to be an input (usually inverting). The operation of the 330 comparator is similar to a digital device in that it has two

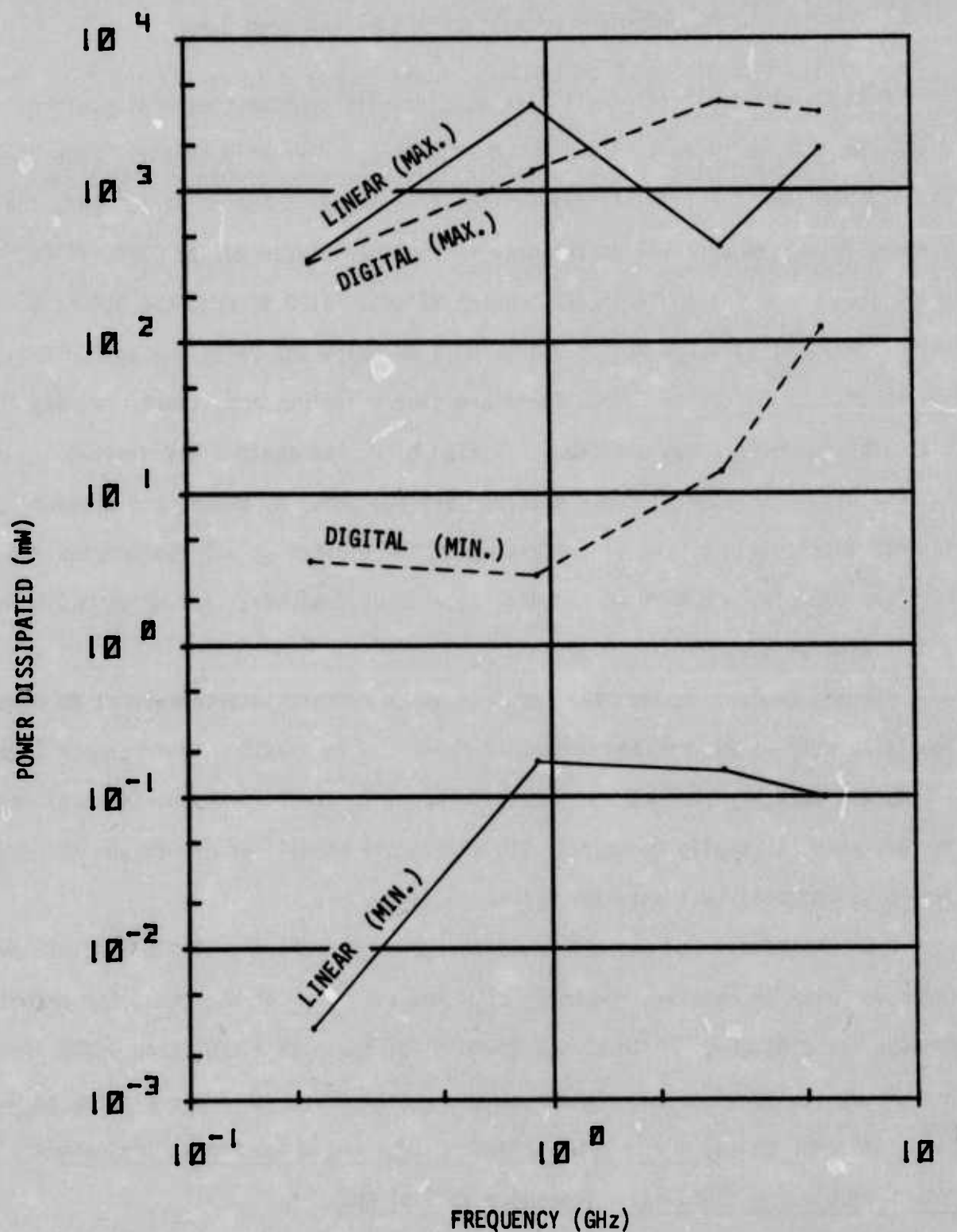


FIGURE 20 LINEAR AND DIGITAL MAXIMUM AND MINIMUM
SUSCEPTIBILITY THRESHOLD LEVELS

stable output states. Review of the data in tables 4 and 8 shows this device to rank very close to the digital device in power required to exceed the interference level.

The effects of time on RF susceptibility have been previously discussed. In general, it is considered that changes in observed RF interference with time may be due to RF heating. These changes with time of RF interference influenced digital devices to a greater degree than linear.

INTEGRATED CIRCUIT SUSCEPTIBILITY

MDC E1126
9 AUGUST 1974

5. CONCLUSIONS AND RECOMMENDATIONS

Both digital and linear devices were tested to determine susceptibility threshold levels and to provide information towards understanding RF effects in bipolar devices. Based on the test conditions used, it may be said that linear devices are generally more susceptible than digital. Outputs on digital devices appear generally to be the most susceptible while inputs are the most susceptible on linear devices. The scope of this task did not permit an in-depth investigation of RF effects on these extra devices at this point. However, it is believed that significant comparisons could be made between these devices and the 7400 and 741 devices. It is recommended that further work include detailed analysis of the RF effects observed in this study. Additional investigation at 0.91 GHz is recommended to determine whether effects may be related to basic device fabrication techniques involving geometry of chip layout which could cause resonance at this frequency. A study of heating effects is necessary to allow RF interference effects to be distinguished from and/or related to temperature effects.

INTEGRATED CIRCUIT SUSCEPTIBILITY

MDC E1126
9 AUGUST 1974

6. REFERENCES

1. "Integrated Circuit Electromagnetic Susceptibility Investigation - MOS NAND Gate Study", MDC Report E1101, dated 26 July 1974. Prepared under contract No. N00178-73-C-0362 for the U. S. Naval Weapons Laboratory by McDonnell Douglas Astronautics Company - East, St. Louis, Missouri 63166
2. "Integrated Circuit Electromagnetic Susceptibility Investigation - Test and Measurement Systems", MDC Report E1099, dated 12 July 1974. Prepared under contract number N00178-73-C-0362 for the U. S. Naval Weapons Laboratory by McDonnell Douglas Astronautics Company - East, St. Louis, Missouri 63166
3. "Integrated Circuit Electromagnetic Susceptibility Investigation - MOS/Hybrid Study", MDC Report E1125, dated 9 August 1974. Prepared under contract number N00178-73-C-0362 for the U. S. Naval Weapons Laboratory by McDonnell Douglas Astronautics Company - East, St. Louis, Missouri 63166
4. "Integrated Circuit Electromagnetic Susceptibility Investigation - Bipolar Op Amp Study", MDC Report E1124, dated 9 August 1974. Prepared under contract number N00178-73-C-0362 for the U. S. Naval Weapons Laboratory by McDonnell Douglas Astronautics Company - East, St. Louis, Missouri 63166
5. "Integrated Circuit Electromagnetic Susceptibility Investigation - Bipolar NAND Gate Study", MDC Report E1123, dated 26 July 1974. Prepared under contract number N00178-73-C-0362 for the U. S. Naval Weapons Laboratory by McDonnell Douglas Astronautics Company - East, St. Louis, Missouri 63166

INTEGRATED CIRCUIT SUSCEPTIBILITY

MDC E1126
9 AUGUST 1974

APPENDIX A
DIGITAL SUSCEPTIBILITY PLOTS

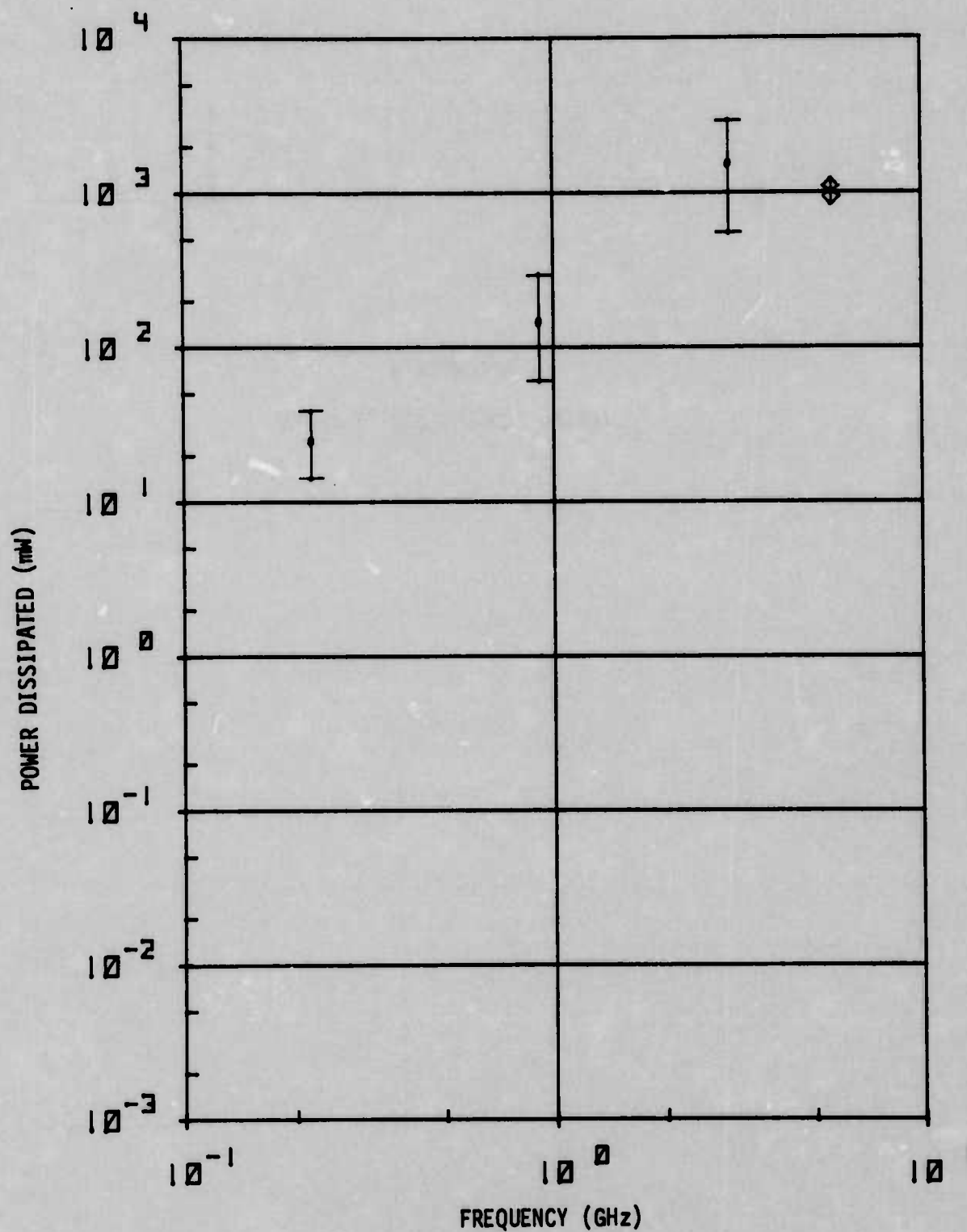


FIGURE A-1 3021 SUSCEPTIBILITY LEVELS
(SAMPLE SIZE = 5)

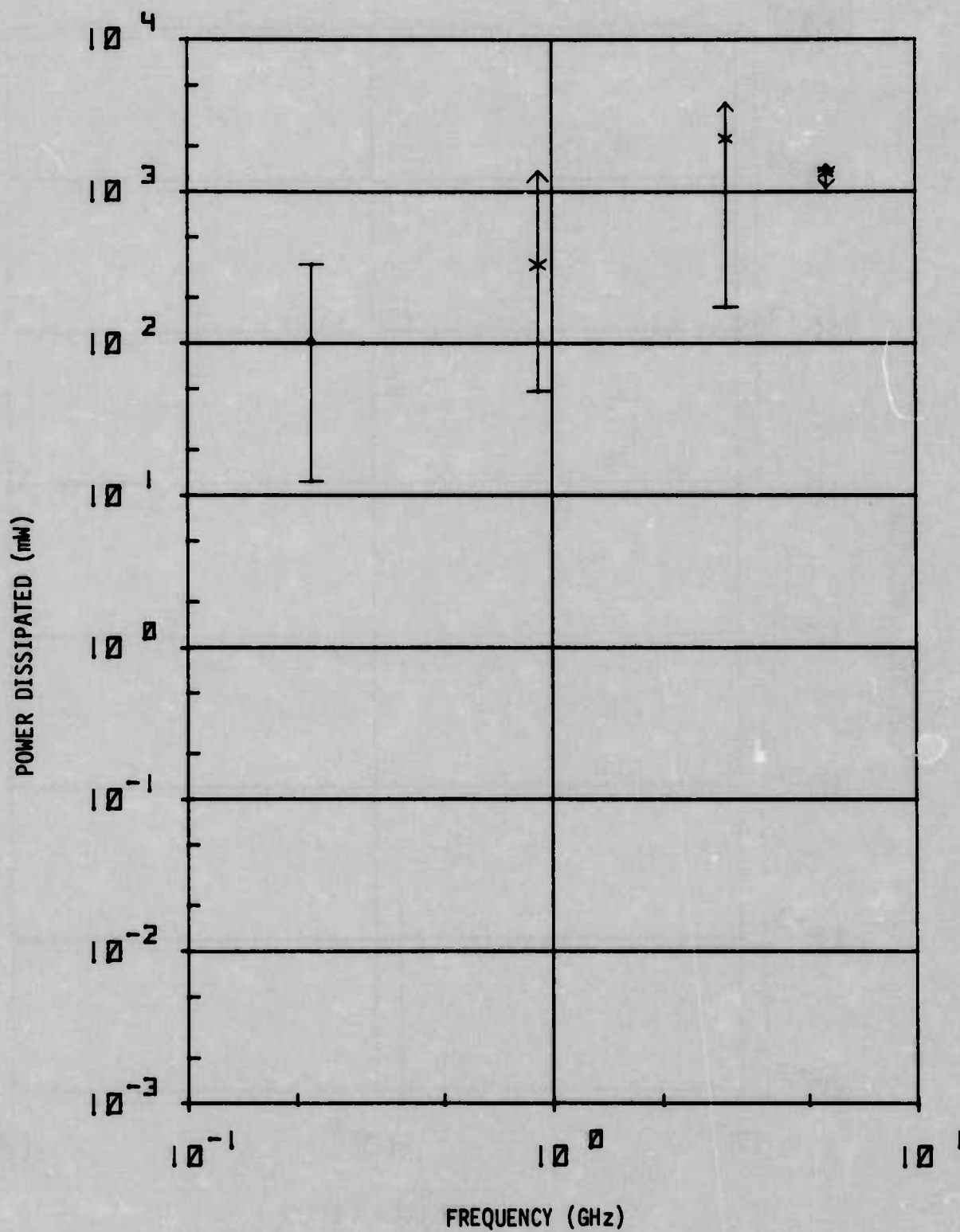


FIGURE A-2 7432 SUSCEPTIBILITY LEVELS
(SAMPLE SIZE = 5)

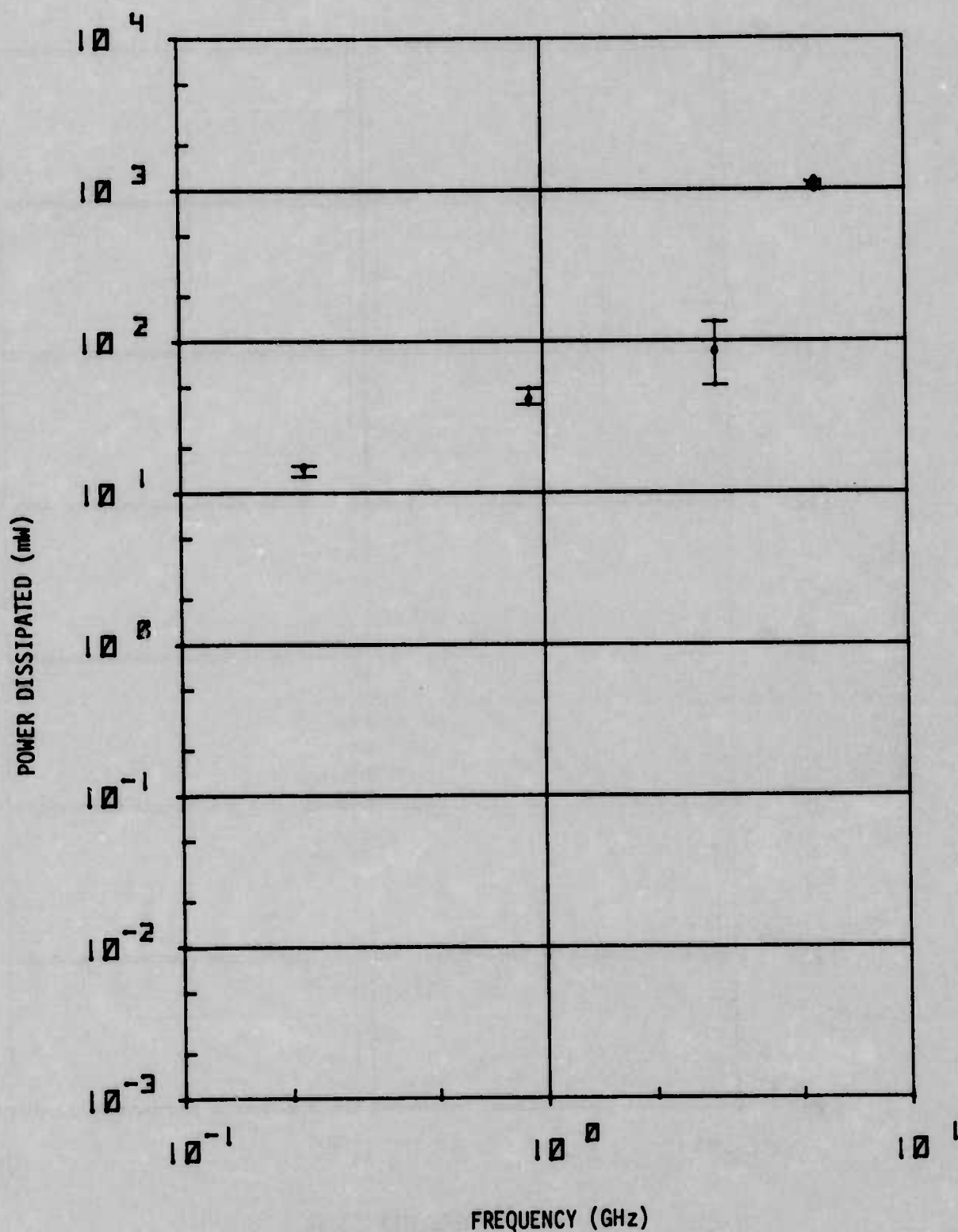


FIGURE A-3 7402 SUSCEPTIBILITY LEVELS
(SAMPLE SIZE = 5)

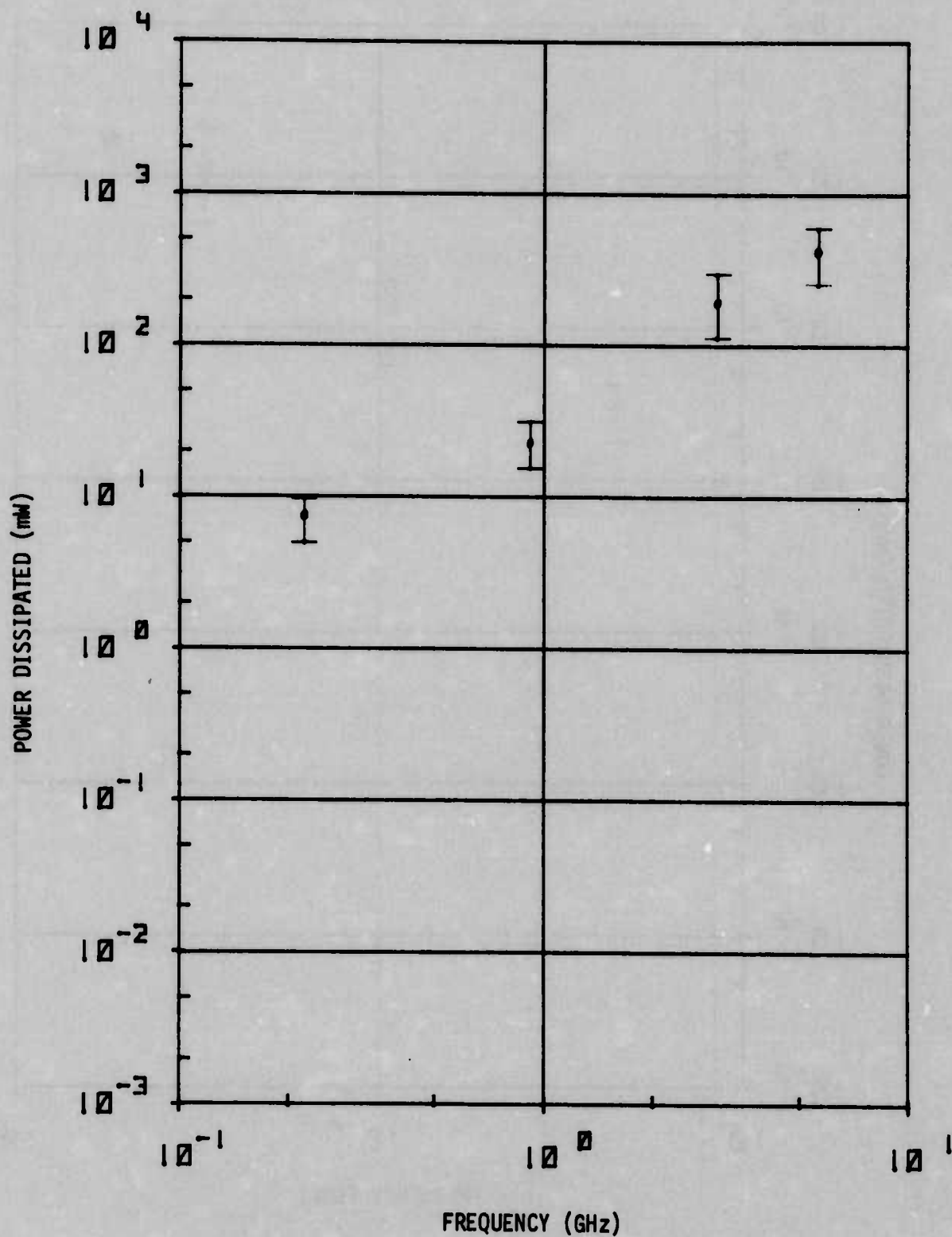


FIGURE A-4 7404 SUSCEPTIBILITY LEVELS
(SAMPLE SIZE = 5)

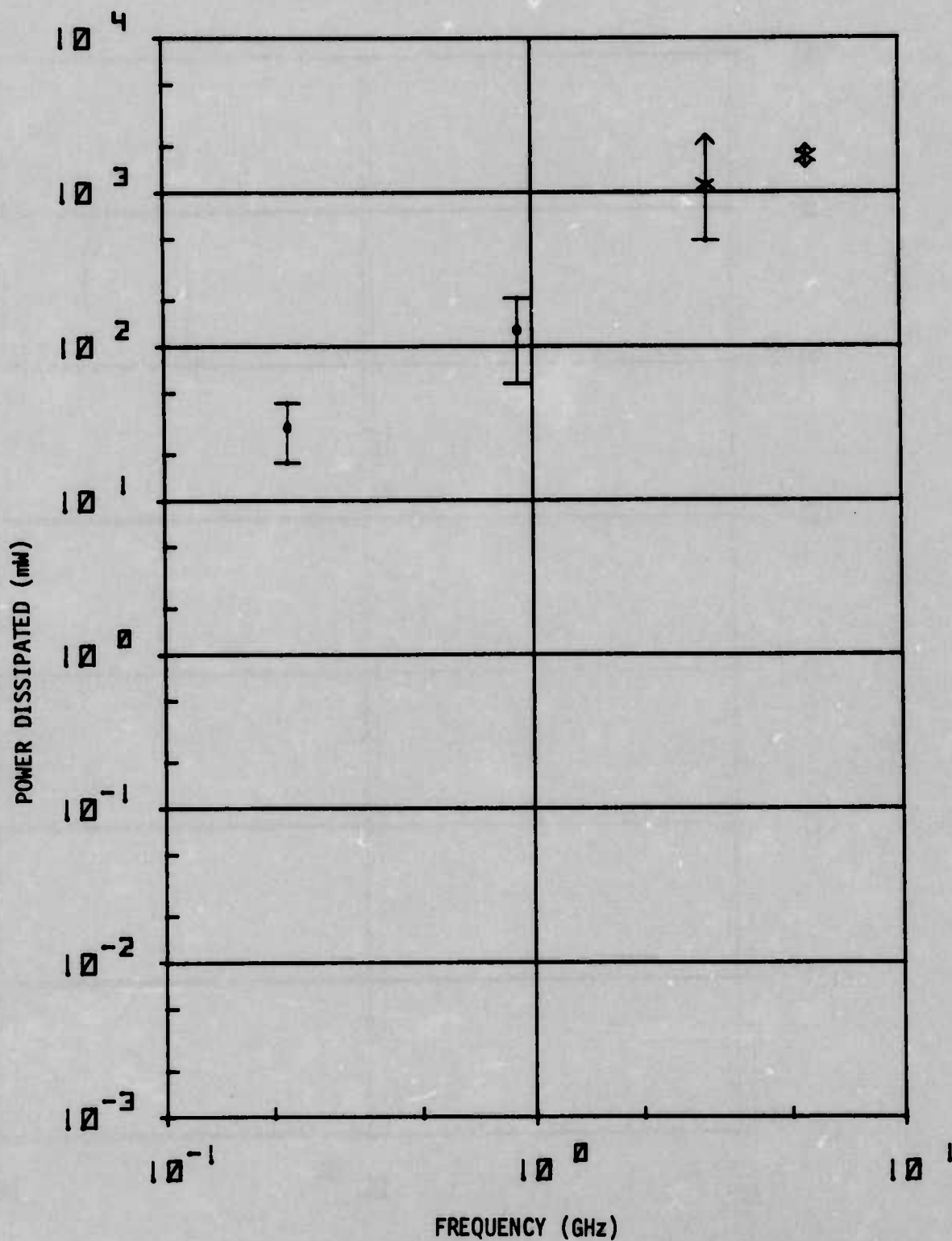


FIGURE A-5 7405 SUSCEPTIBILITY LEVELS
(SAMPLE SIZE = 5)

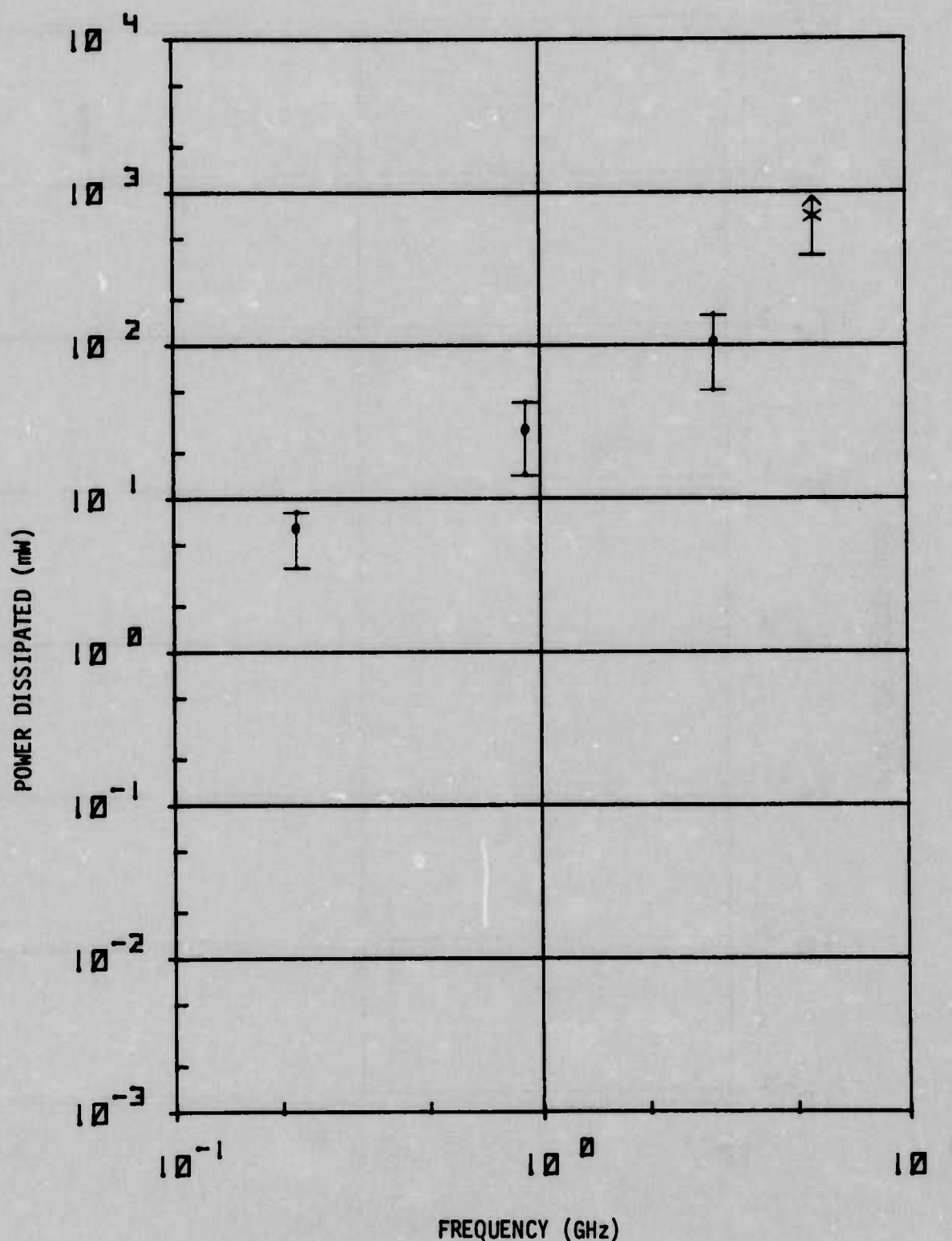


FIGURE A-6 7450 SUSCEPTIBILITY LEVELS
(SAMPLE SIZE = 5)

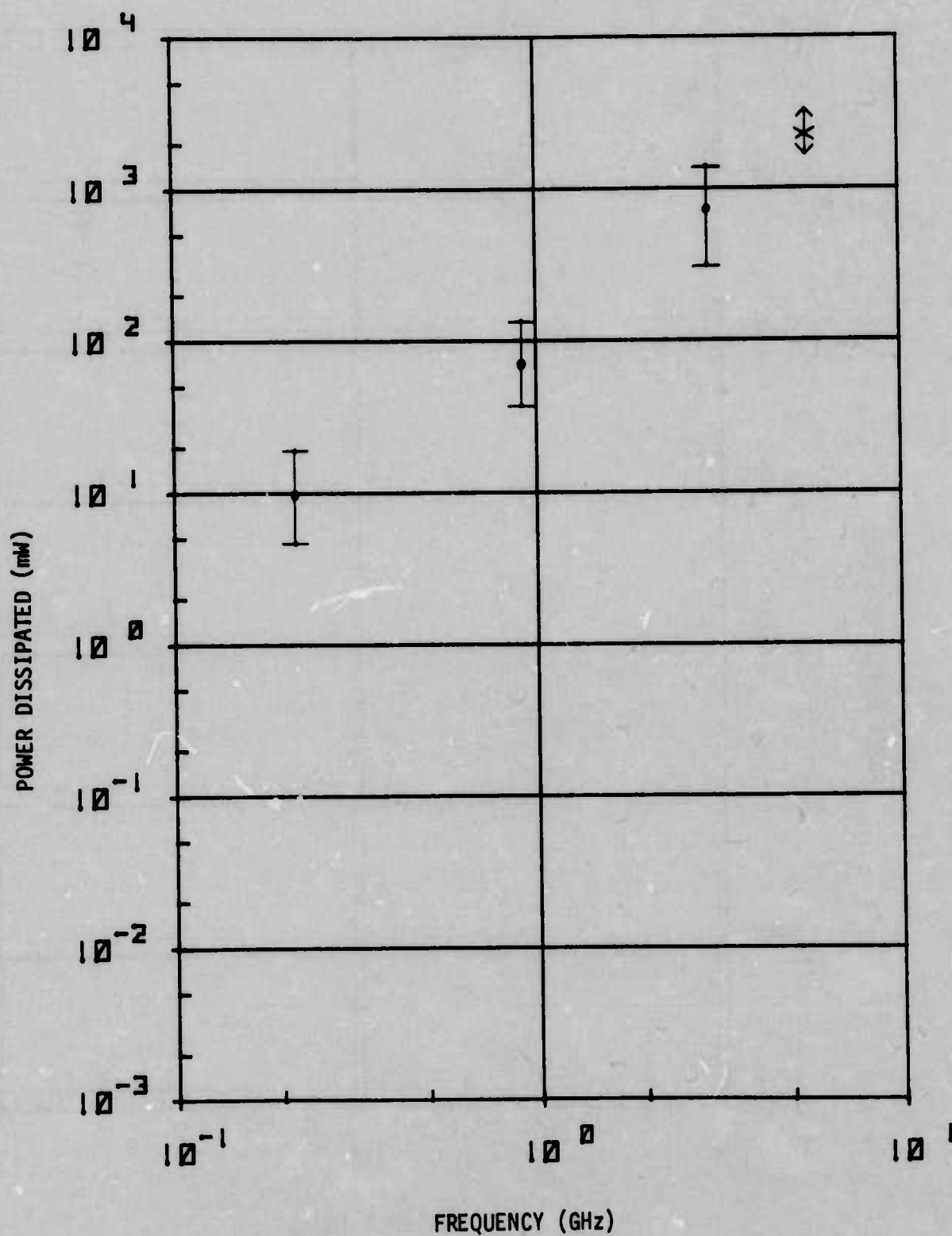


FIGURE A-7 7473 SUSCEPTIBILITY LEVELS
(SAMPLE SIZE = 5)

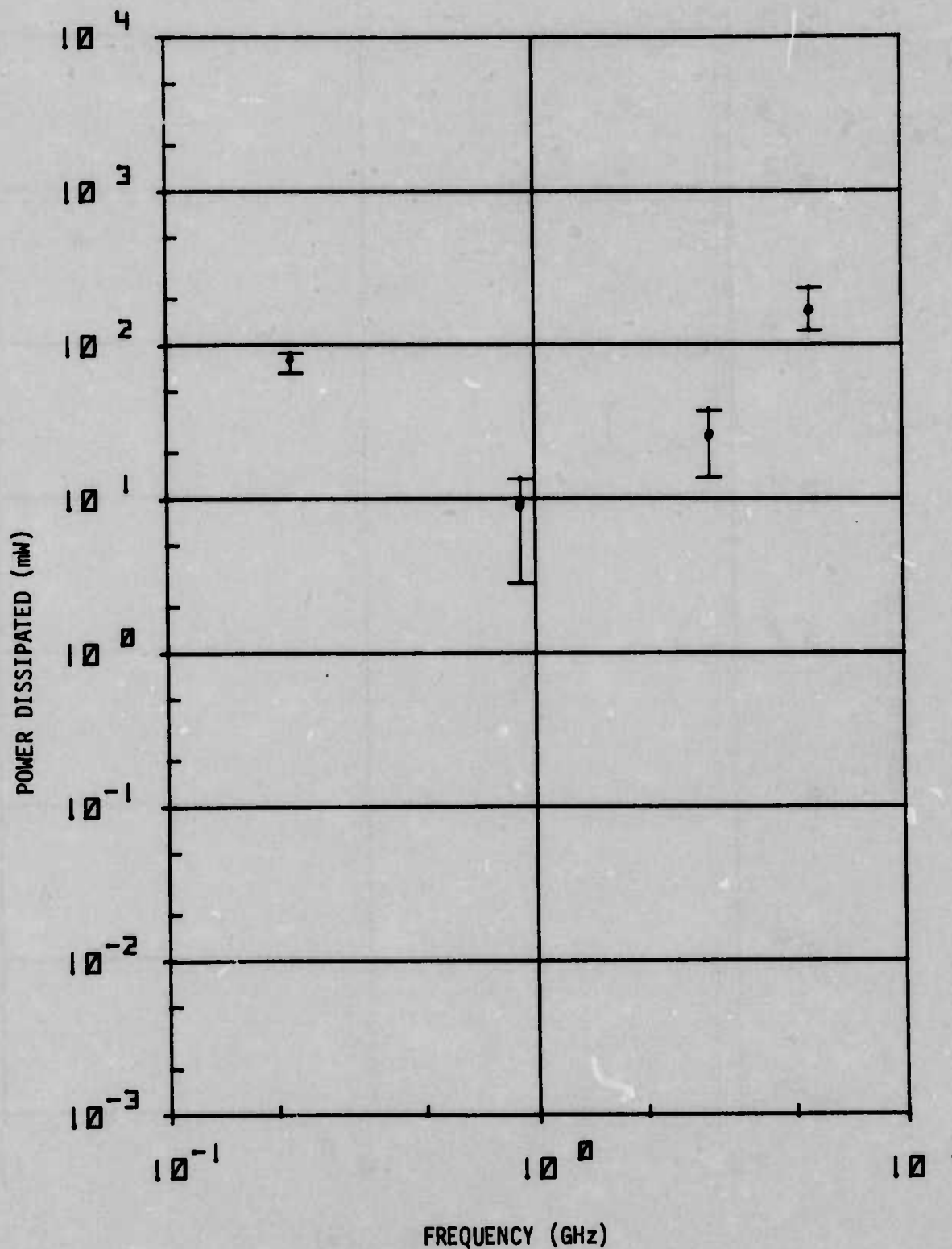


FIGURE A-8 7479 SUSCEPTIBILITY LEVELS
(SAMPLE SIZE = 5)

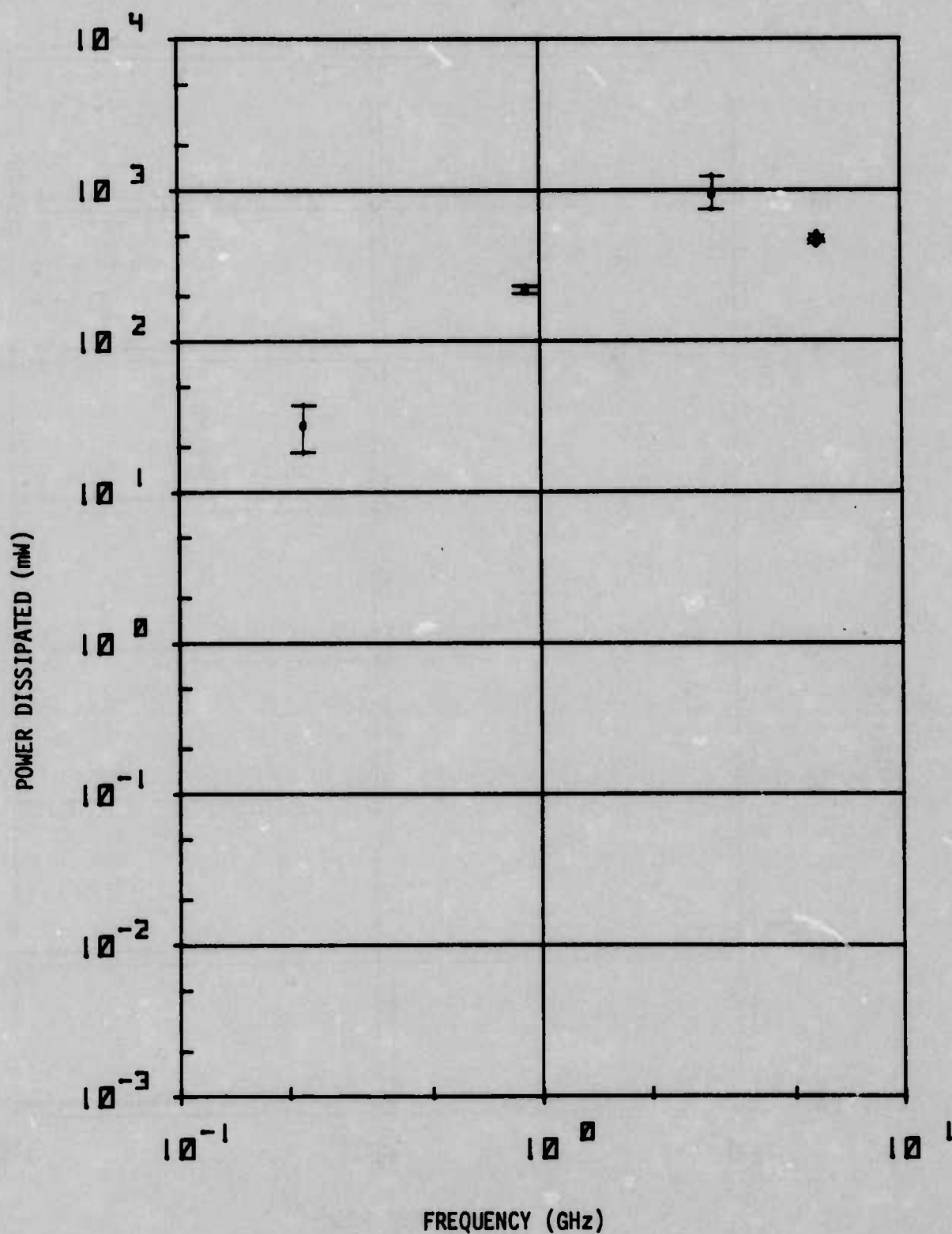


FIGURE A-9 4011 SUSCEPTIBILITY LEVELS
(SAMPLE SIZE = 5)

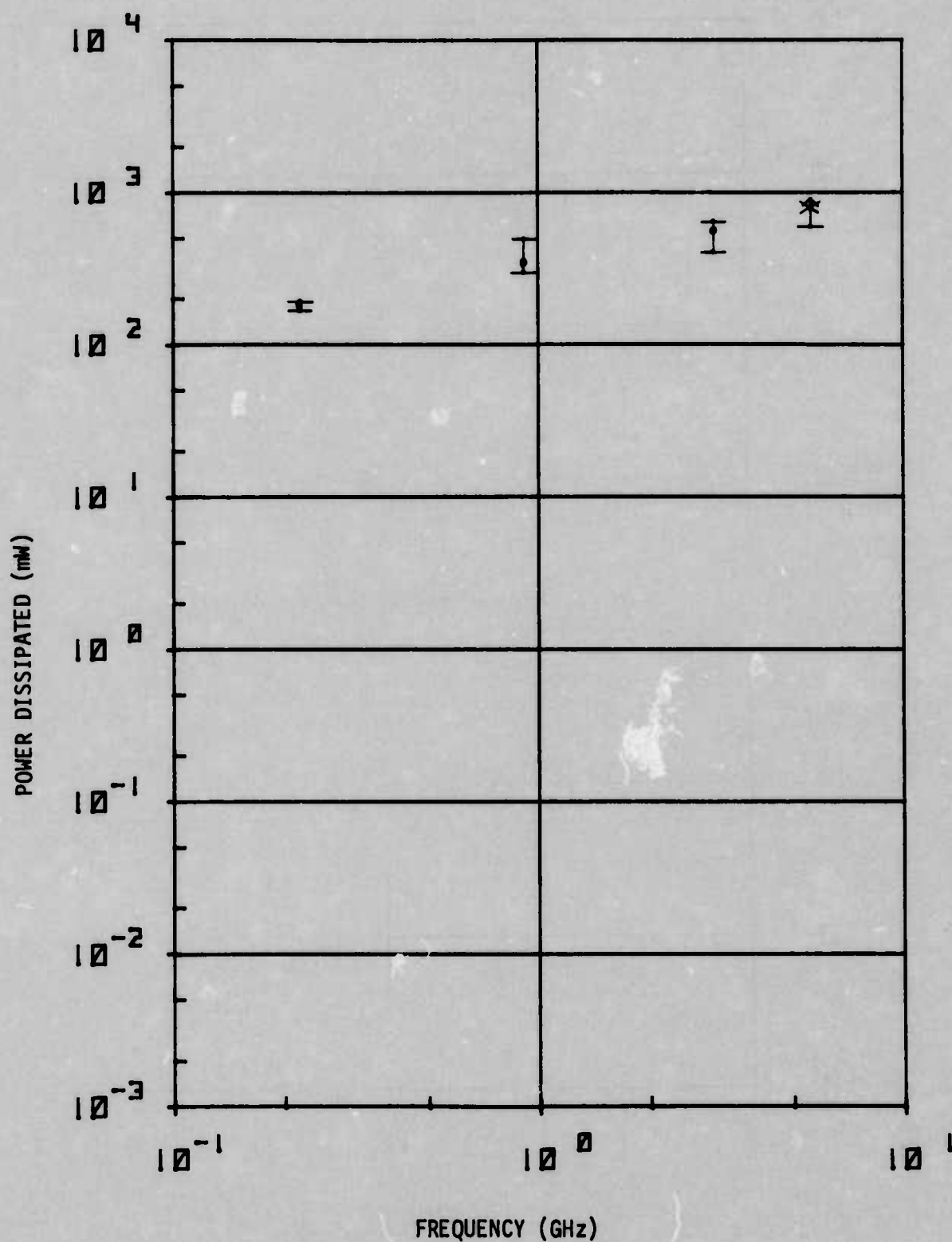


FIGURE A-10 2002 SUSCEPTIBILITY LEVELS

(SAMPLE SIZE = 5)

INTEGRATED CIRCUIT SUSCEPTIBILITY

MDC E1126
9 AUGUST 1974

APPENDIX B
DIGITAL SUSCEPTIBILITY DATA

INTEGRATED CIRCUIT SUSCEPTIBILITY

MDC E1126
9 AUGUST 1974

FIGURE B-1 SUSCEPTIBILITY THRESHOLD LEVELS FOR DIGITAL DEVICE SAMPLE
(SAMPLE SIZE = 5)

DEVICE NUMBER	SUSCEPTIBILITY THRESHOLD LEVEL (mW)							
	0.22 GHz		0.91 GHz		3.0 GHz		5.6 GHz	
3021	16.8 29.8 14.4	26.3 39.0	73.6 156.7 61.0	162.4 293.3	1051.9 2447.9 550.2	2938.0 919.9	*840.9 *931.1 *1211.8	*1023.6 *1080.1
7432	12.6 118.2 21.8	36.8 331.6	207.2 *1340.1 48.8	52.3 343.6	*3472.3 *3806.8 177.1	250.8 *3591.0	*1423.3 *1271.4 *1473.2	*1092.9 *1534.8
7402	15.3 13.2 15.5	15.5 15.1	44.1 38.5 49.1	40.6 39.4	133.4 61.9 67.0	121.3 51.6	*1175.7 * 997.8 *1037.3	*1063.6 * 984.0
7404	9.8 7.0 5.0	9.0 6.7	30.9 23.2 15.5	25.4 19.7	295.6 185.6 114.1	181.9 183.3	589.3 337.0 255.0	528.0 353.6
7405	28.9 18.6 17.7	43.0 38.9	116.3 72.0 58.1	203.9 188.2	*2306.2 966.5 488.5	*1162.8 704.1	*1773.3 *1770.5 *1706.3	*1479.1 *1979.3
7450	3.6 8.3 6.8	7.8 5.9	14.6 41.3 25.4	42.6 19.0	51.5 151.0 104.7	157.6 69.4	526.6 * 906.3 735.3	* 906.3 389.7
7473	19.4 6.9 10.7	7.9 4.7	133.7 50.8 73.8	58.2 37.6	1405.7 504.3 844.2	607.7 312.7	*2398.0 *2330.4 *1856.6	*1702.4 *3228.1
7479	86.0 67.4 85.0	77.5 89.9	8.9 10.0 13.7	9.8 2.9	26.4 21.3 14.1	31.8 37.9	163.4 154.4 124.5	159.1 232.3
4011	18.5 21.0 25.0	36.0 38.0	210.0 220.0 215.0	225.0 230.0	850.0 1250.0 925.0	900.0 750.0	* 437.8 * 512.3 * 444.8	* 504.8 * 532.4
2002	180.0 194.0 181.0	186.0 168.0	494.0 311.0 316.0	322.0 301.0	600.2 634.0 505.0	641.0 407.0	* 810.0 * 887.0 * 596.0	741.0 * 881.0

* - INDICATES MAXIMUM RF POWER LEVEL APPLIED WITH NO SUSCEPTIBILITY THRESHOLD REACHED

APPENDIX C
LINEAR SUSCEPTIBILITY PLOTS

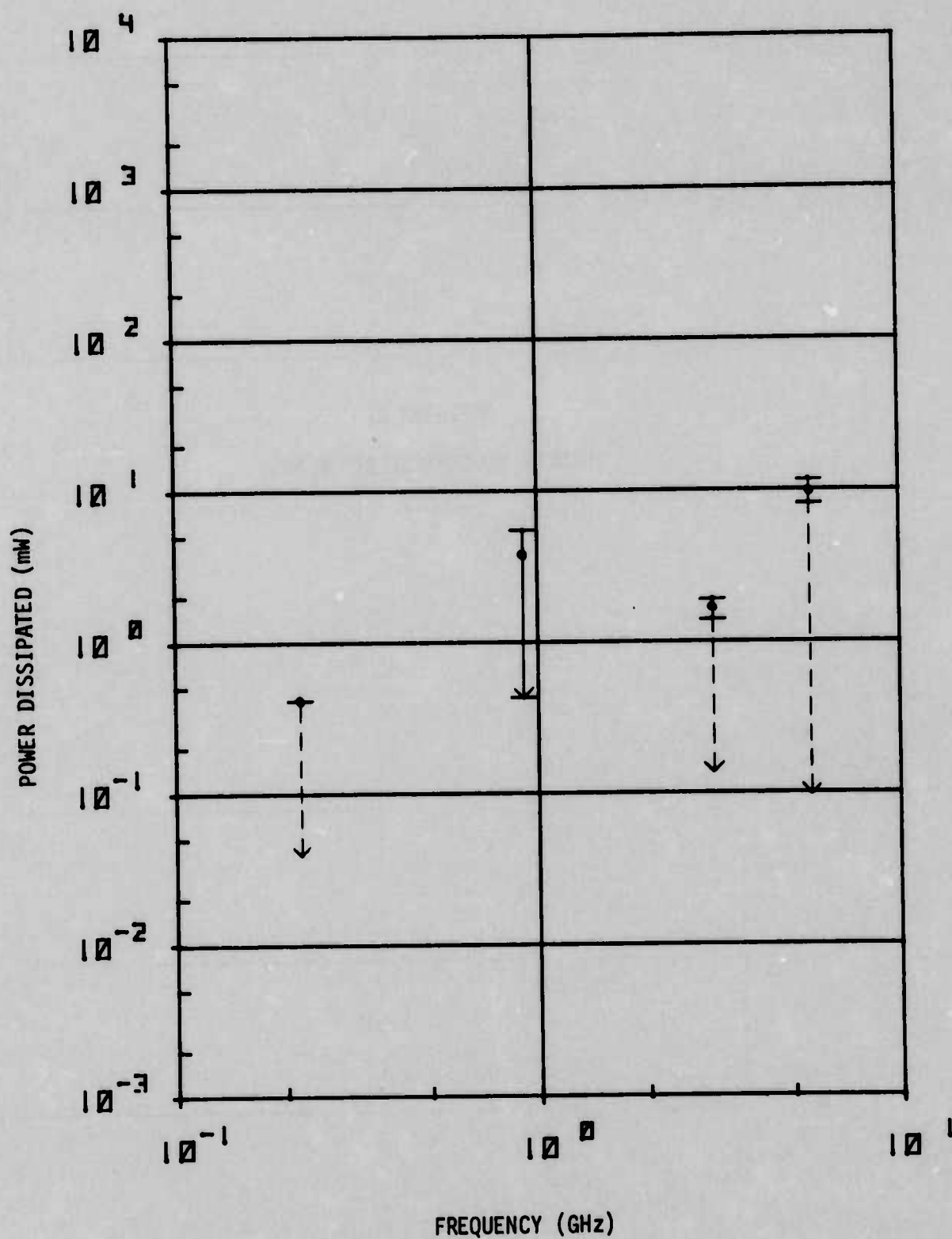


FIGURE C-1 201 SUSCEPTIBILITY LEVELS
(SAMPLE SIZE = 5)

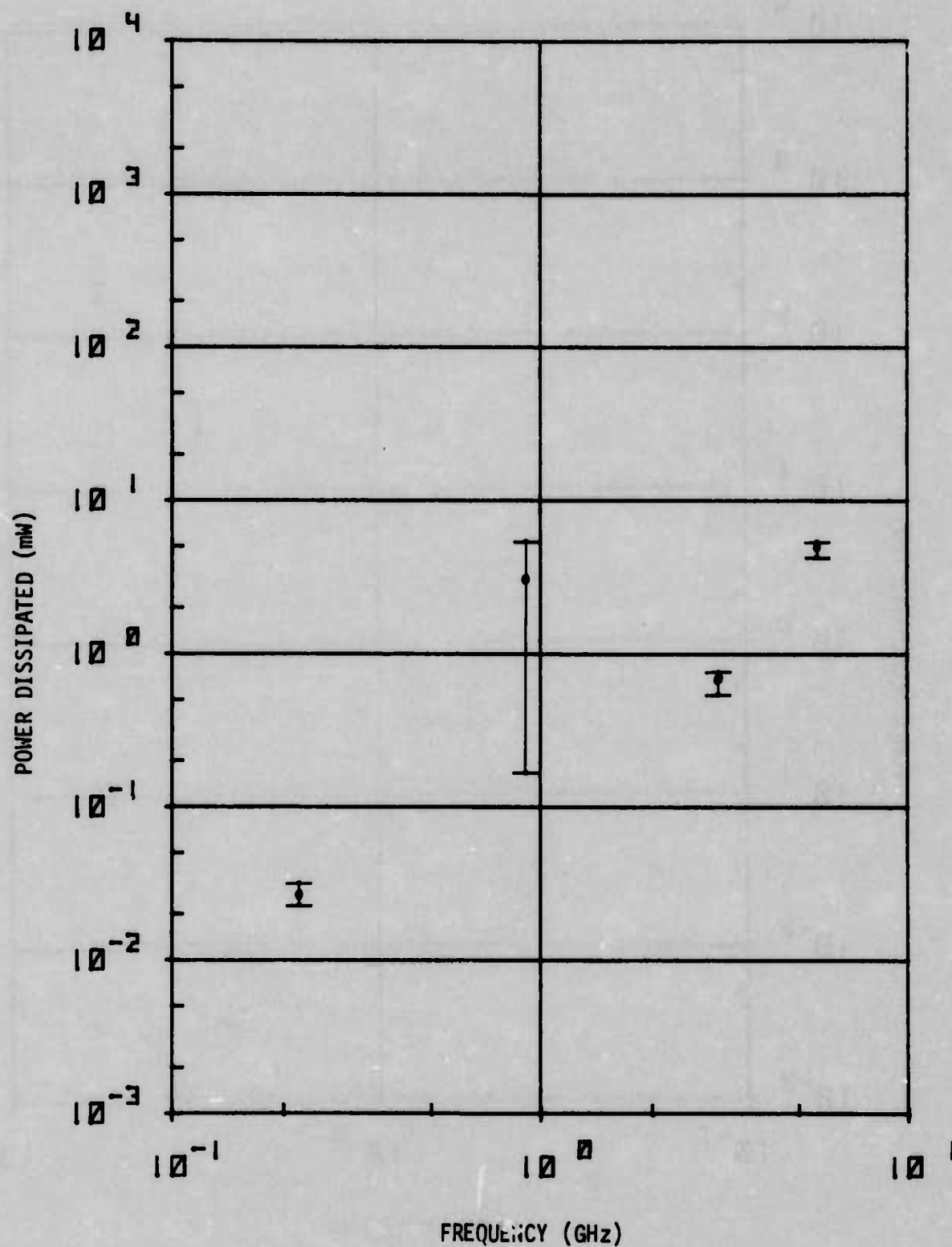


FIGURE C-2 307 SUSCEPTIBILITY LEVELS
(SAMPLE SIZE = 5)

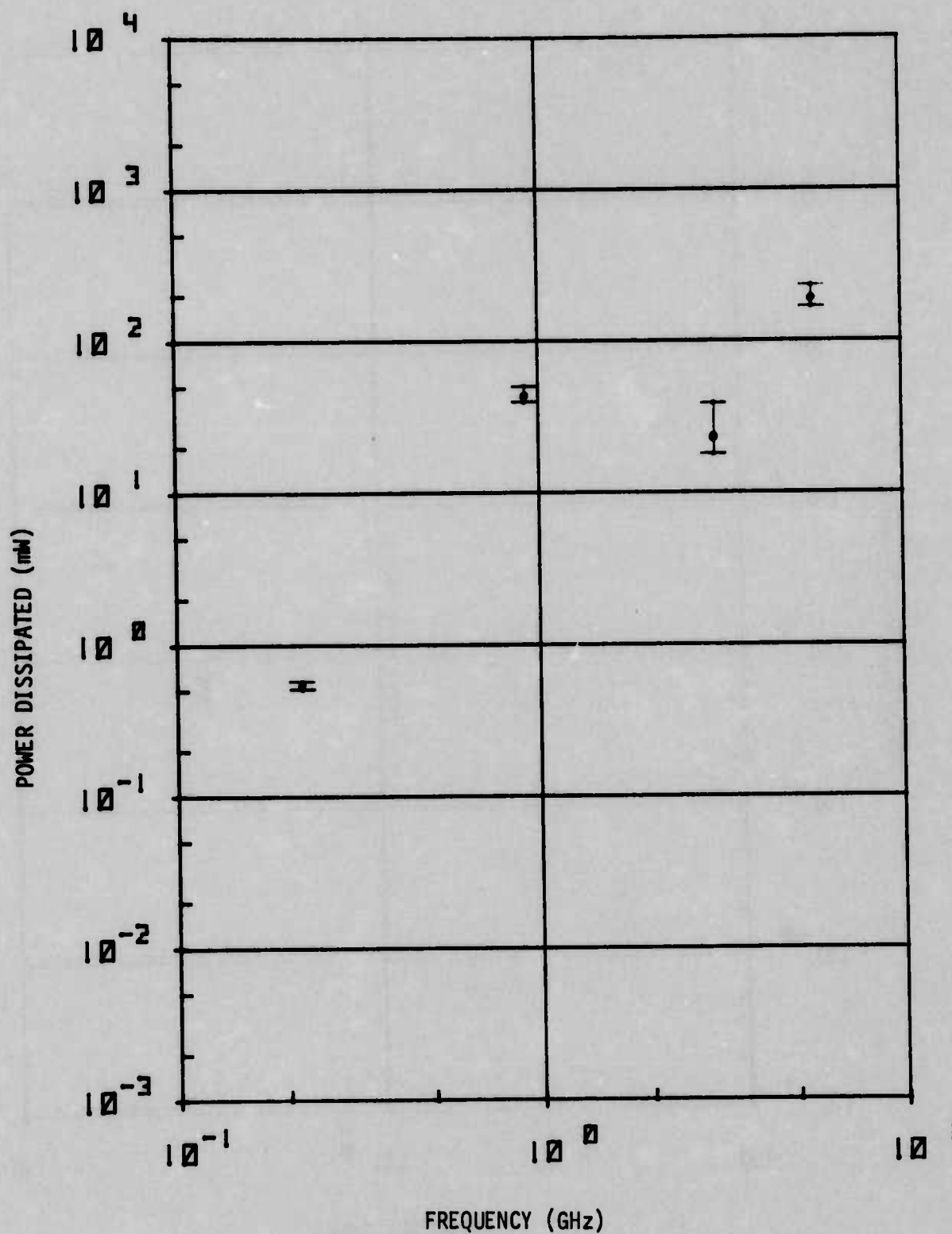


FIGURE C-3 310 SUSCEPTIBILITY LEVELS
(SAMPLE SIZE = 5)

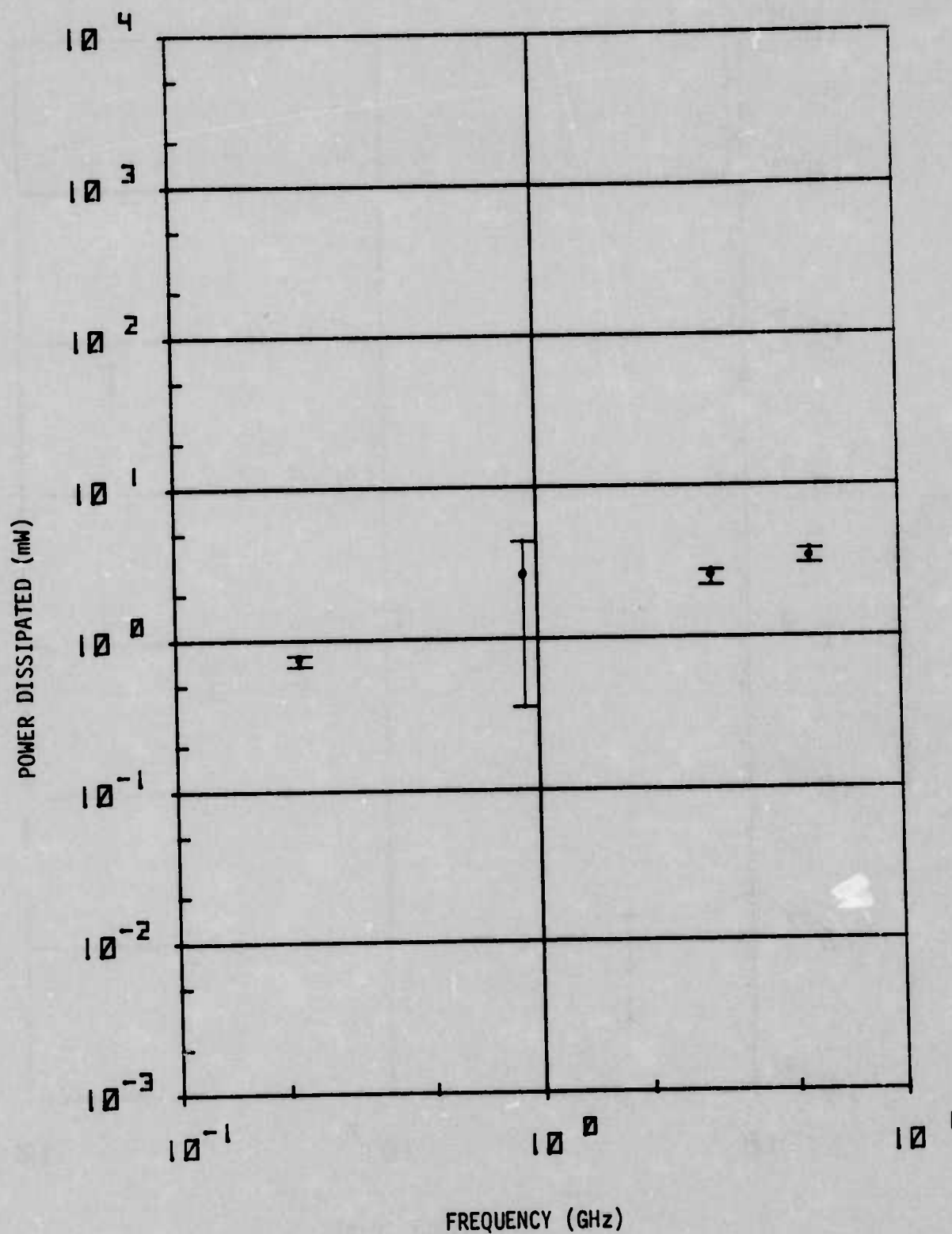


FIGURE C-4 316 SUSCEPTIBILITY LEVELS
(SAMPLE SIZE = 5)

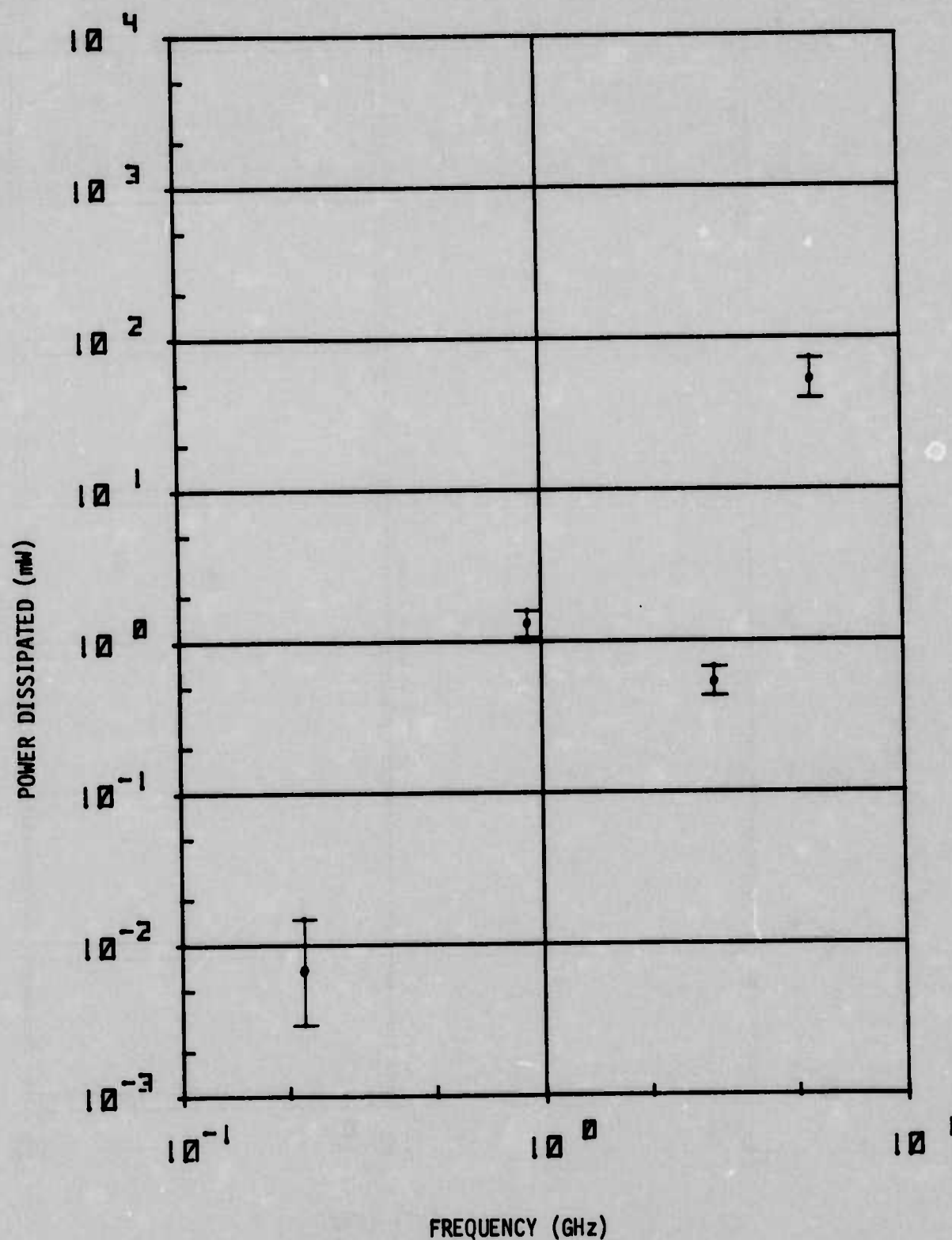


FIGURE C-5 324 SUSCEPTIBILITY LEVELS
(SAMPLE SIZE = 5)

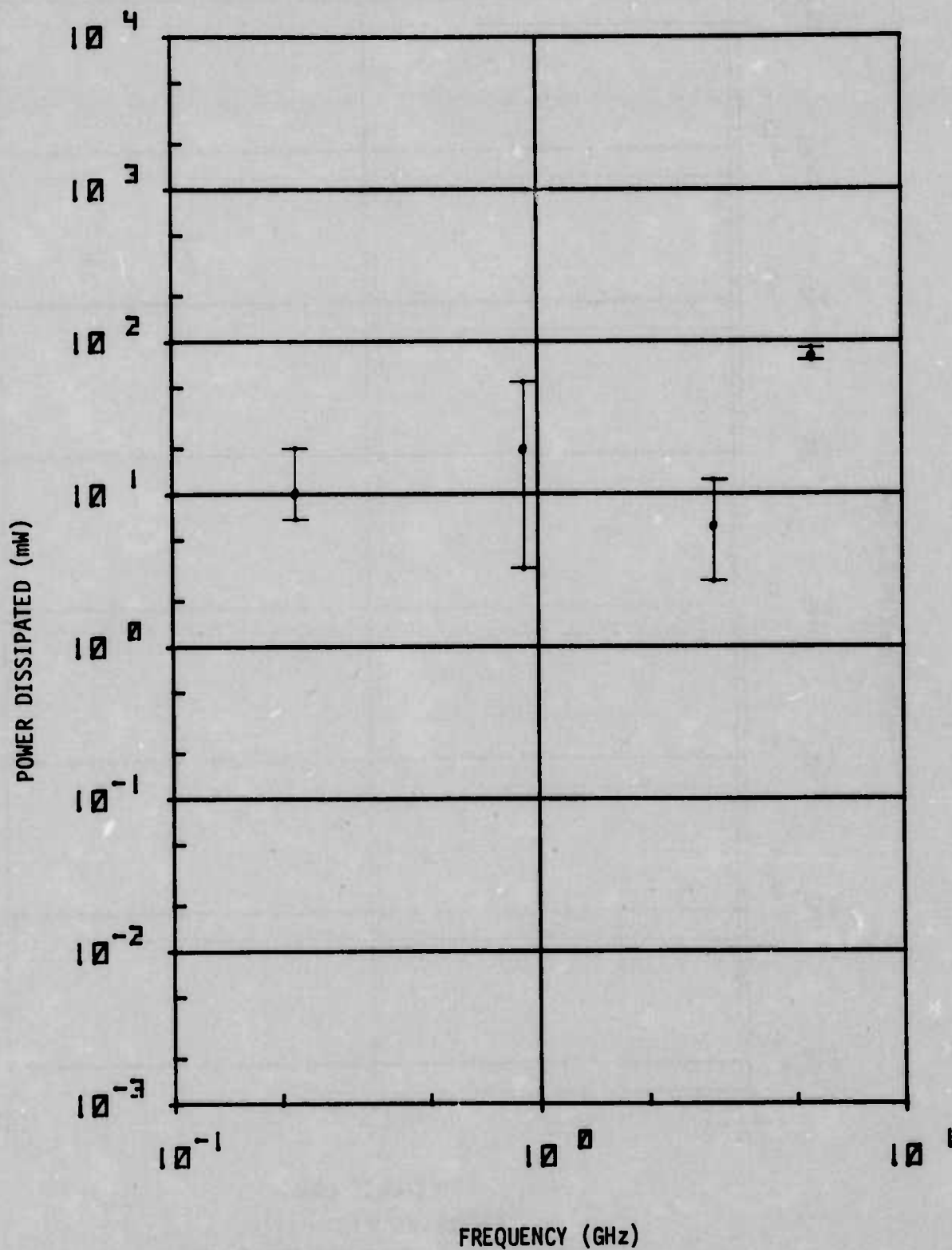


FIGURE C-6 339 SUSCEPTIBILITY LEVELS

(SAMPLE SIZE = 5)

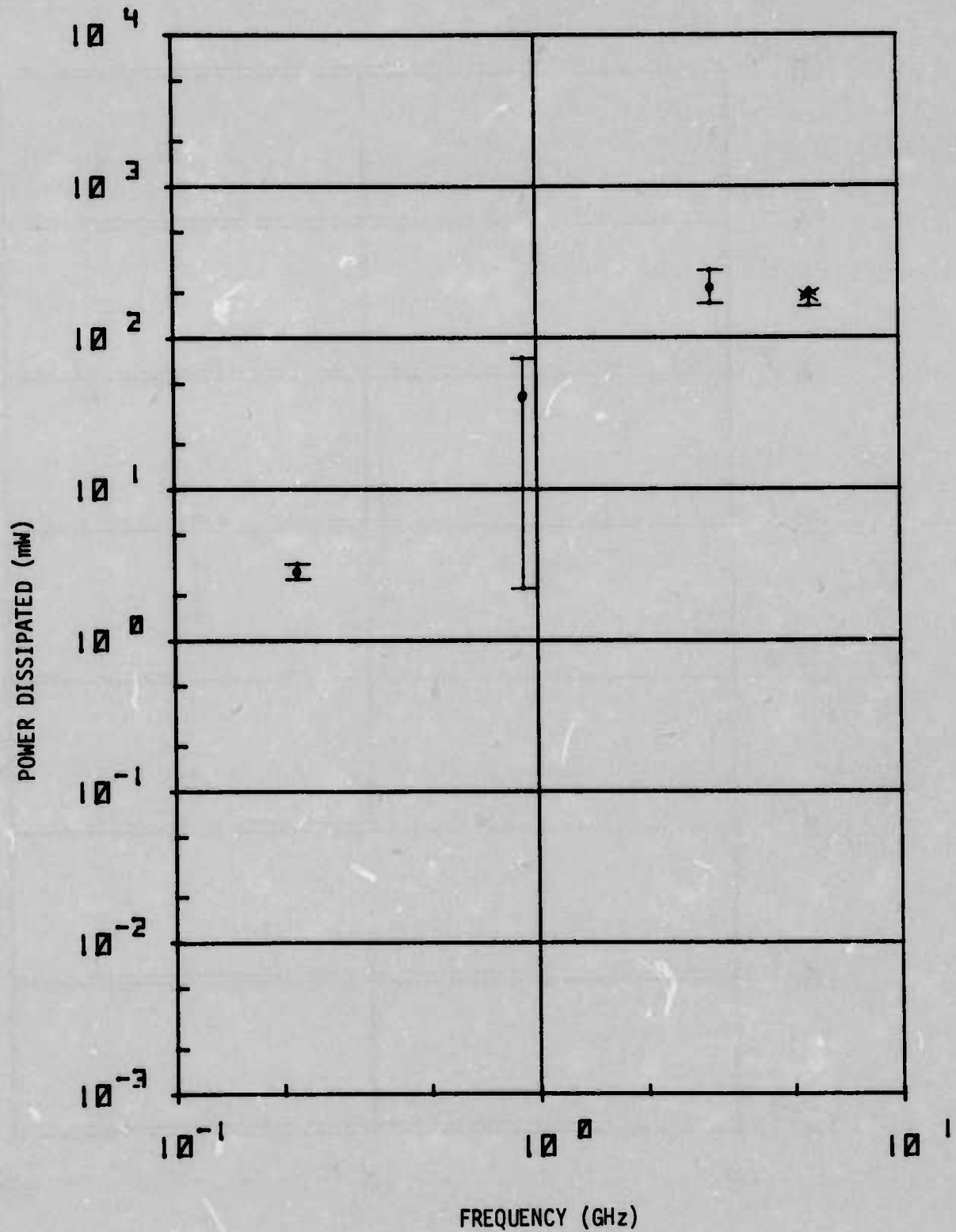


FIGURE C-7 725 SUSCEPTIBILITY LEVELS

(SAMPLE SIZE = 5)

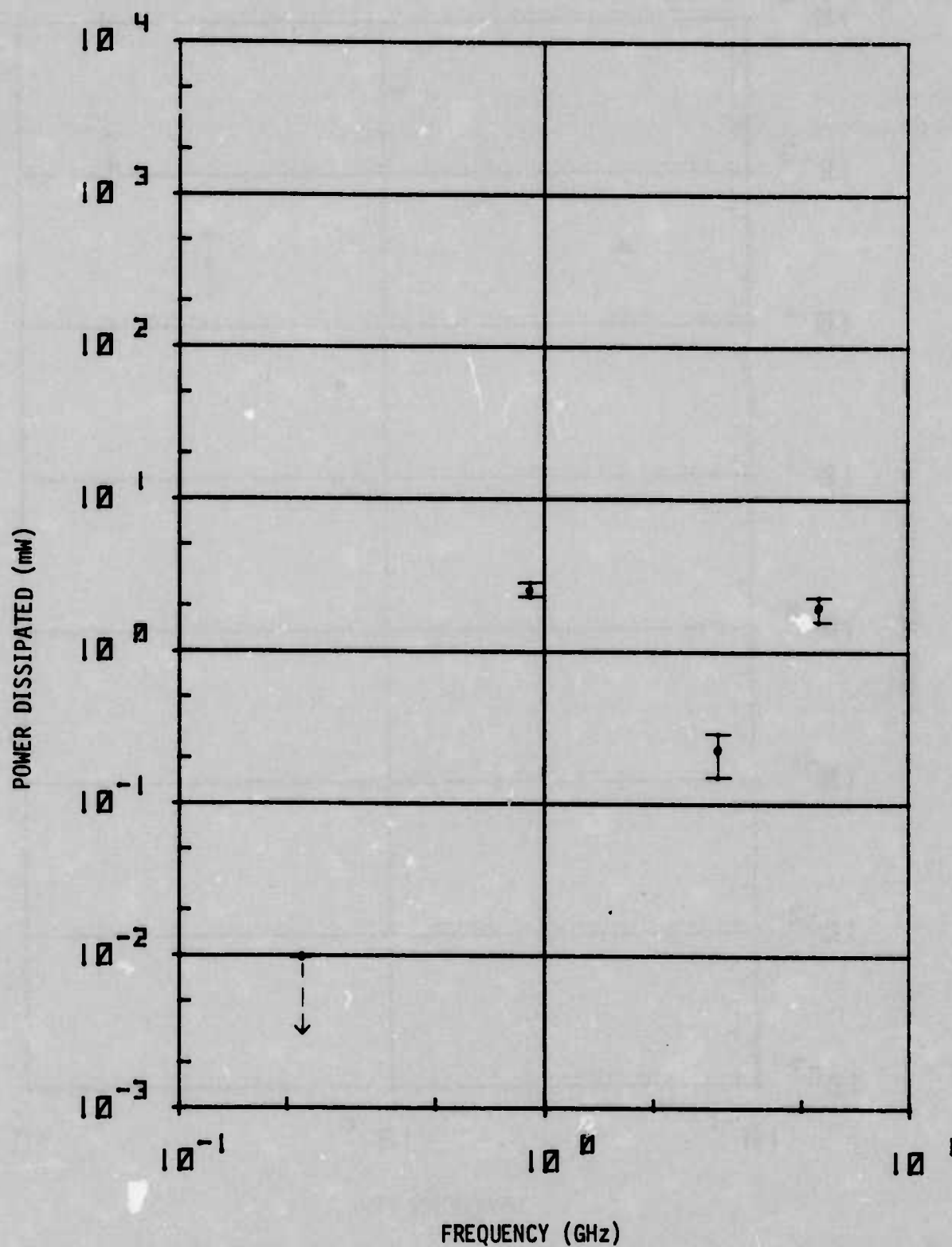


FIGURE C-8 747 SUSCEPTIBILITY LEVELS
(SAMPLE SIZE = 5)

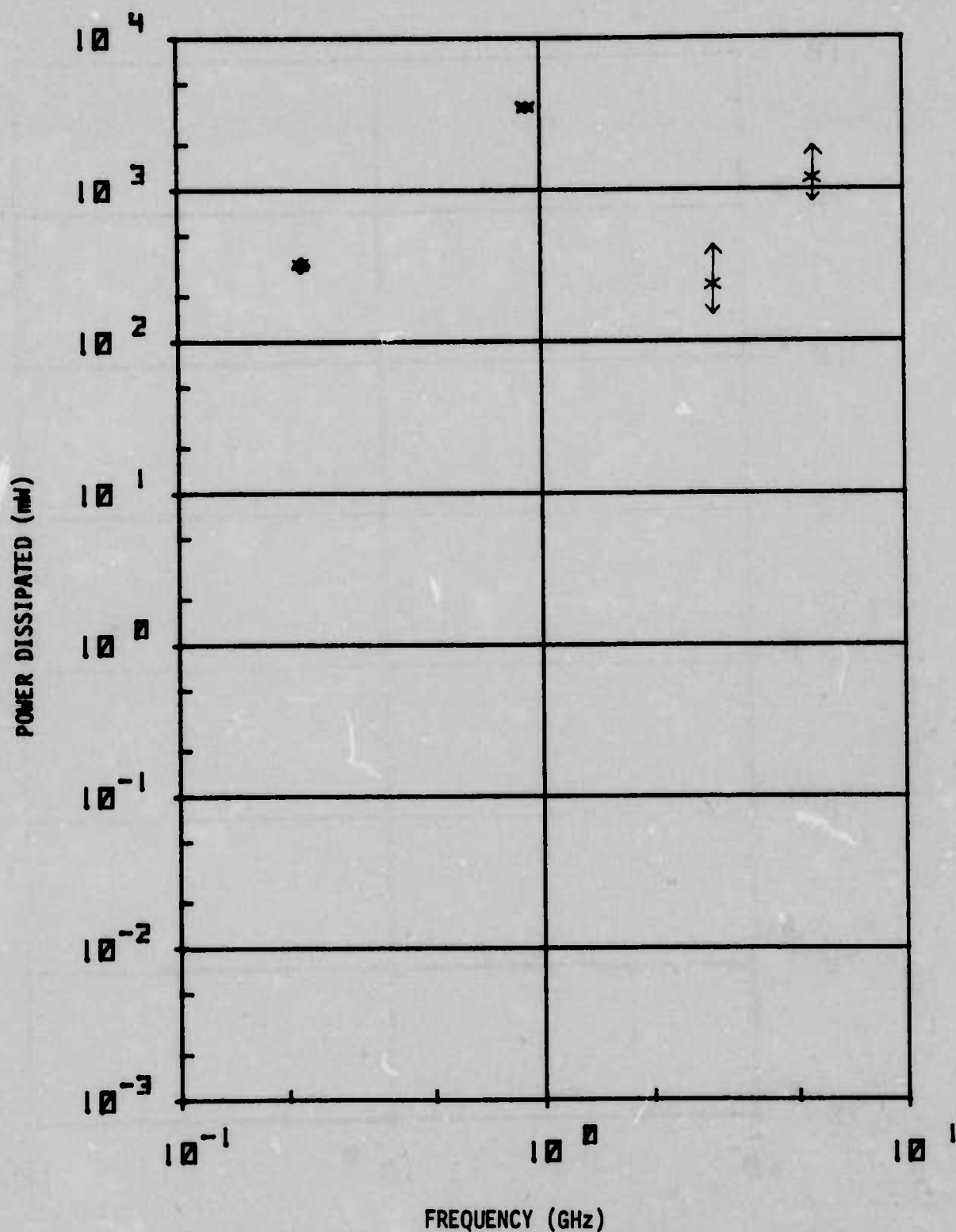


FIGURE C-9 309 SUSCEPTIBILITY LEVELS
(SAMPLE SIZE = 5)

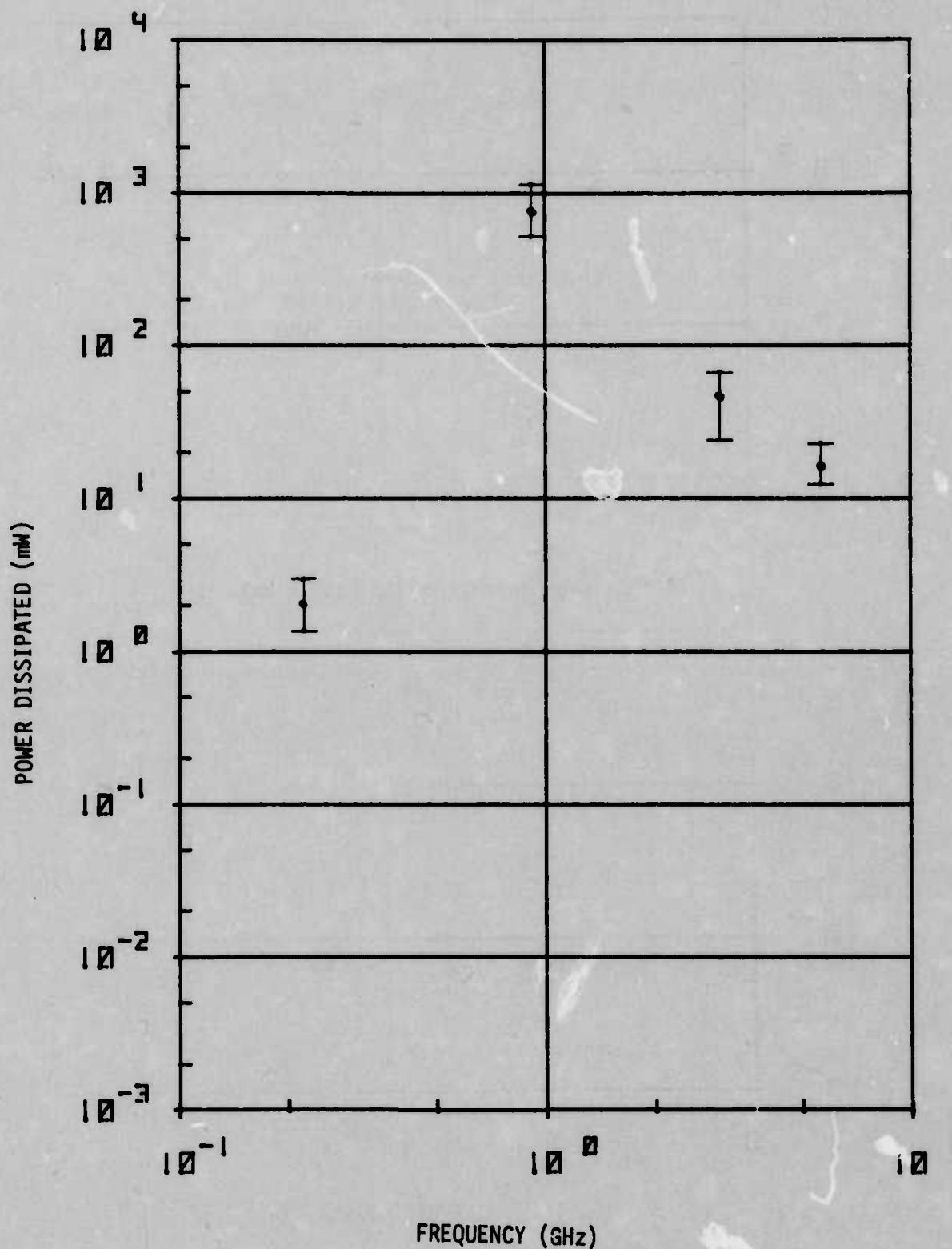


FIGURE C-10 320 SUSCEPTIBILITY LEVELS

(SAMPLE SIZE = 5)

PRECEDING PAGE BLANK-NOT FILMED

APPENDIX D
LINEAR SUSCEPTIBILITY DATA

INTEGRATED CIRCUIT SUSCEPTIBILITY

MDC E1126
9 AUGUST 1974

DEVICE SN. NO.	SUSCEPTIBILITY THRESHOLD LEVEL (mW)							
	0.22 GHz		0.91 GHz		3.0 GHz		5.6 GHz	
309	*297.7 *346.7 *350.4	*295.1 *348.2	*3653.8 *3459.3 *3657.6	*3328.7 *3561.7	* 44.4 * 354.4 * 226.0	* 156.1 * 420.0	*1218.7 *1131.7 *1864.8	* 854.5 * 910.4
725	2.67 3.08 2.79	2.60 3.25	72.90 72.50 2.84	55.60 2.25	246.5 168.3 195.0	274.4 181.4	* 184.1 * 184.0 * 205.0	* 162.1 * 196.1
320	1.67 2.96 2.32	1.93 1.38	548.2 1135.9 788.2	775.7 524.9	24.3 38.2 67.8	55.7 47.2	22.9 16.9 12.8	12.5 15.3
747	0.01 0.01 0.01	0.01 ⁺ 0.01	2.66 2.43 2.58	2.81 2.30	0.29 0.26 0.25	0.19 0.15	2.15 2.20 2.25	1.56 1.65
201	0.41 0.42 0.42	0.42 0.42	0.44 4.98 4.43	3.79 5.43 _Δ	1.68 1.76 1.90	1.59 1.41 _Δ	9.2 10.5 11.6	8.5 8.1 _Δ
307	0.023 0.031 0.032	0.023 0.027	5.39 0.17 0.18	4.71 4.97	0.76 0.55 0.76	0.68 0.73	5.37 4.83 5.13	4.33 5.31
316	0.68 0.72 0.78	0.75 0.79	3.90 0.36 0.39	4.37 4.34	2.24 2.71 2.54	2.67 2.76	3.08 3.17 3.21	3.63 3.80
324	0.015 0.005 0.005	0.003 0.006	1.58 1.07 1.55	1.29 1.21	0.68 0.44 0.50	0.60 0.49	55.8 39.6 48.4	72.6 48.9
339	7.50 9.43 20.20	7.17 6.90	16.40 4.88 53.80	3.27 20.10	12.30 6.51 2.71	4.80 4.94	83.8 90.2 75.2	75.6 77.0
310	0.57 0.58 0.51	0.52 0.55	49.9 45.4 41.6	39.4 42.6	38.4 22.5 18.0	19.4 18.6	171.6 205.6 171.4	167.0 228.5

- + - INDICATES ACTUAL SUSCEPTIBILITY THRESHOLD LEVEL OBTAINED WITH 5 dB LESS INCIDENT RF POWER
* - INDICATES MAXIMUM RF POWER LEVEL APPLIED WITH NO SUSCEPTIBILITY THRESHOLD REACHED
Δ - INDICATES CW SUSCEPTIBILITY THRESHOLD, PULSED APPROXIMATELY 10 dB LOWER

FIGURE D-1 SUSCEPTIBILITY THRESHOLD LEVELS FOR LINEAR DEVICE SAMPLES
(SAMPLE SIZE = 5)

APPENDIX E

CIRCUIT DIAGRAMS
OF DEVICES TESTED

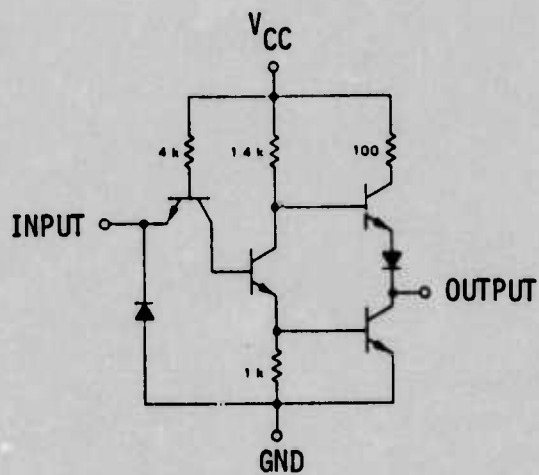


FIGURE E-1 7404 CIRCUIT DIAGRAM

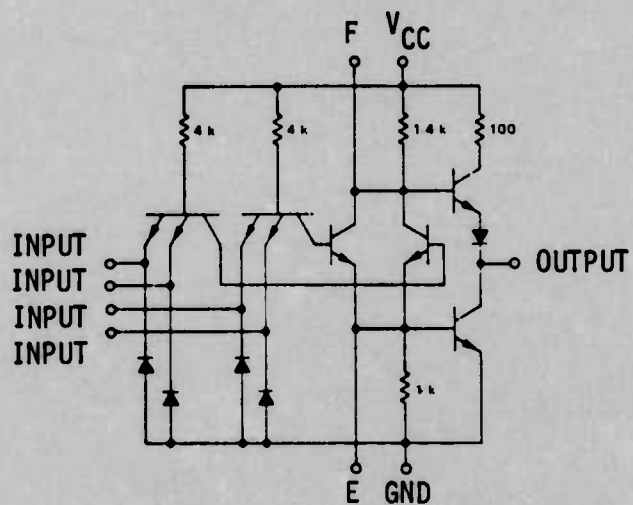


FIGURE E-2 7450 CIRCUIT DIAGRAM

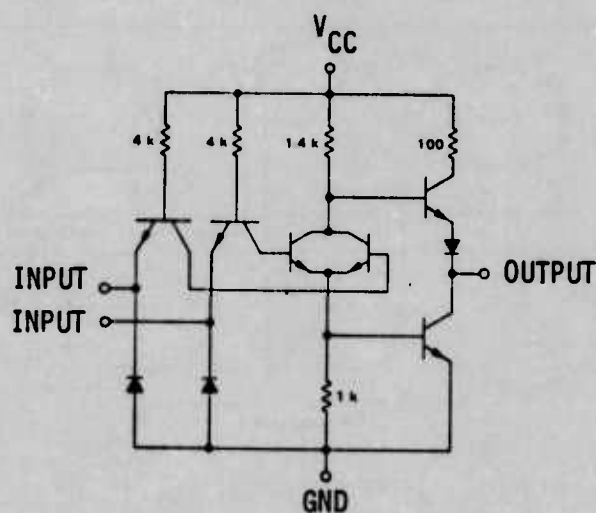


FIGURE E-3 7402 CIRCUIT DIAGRAM

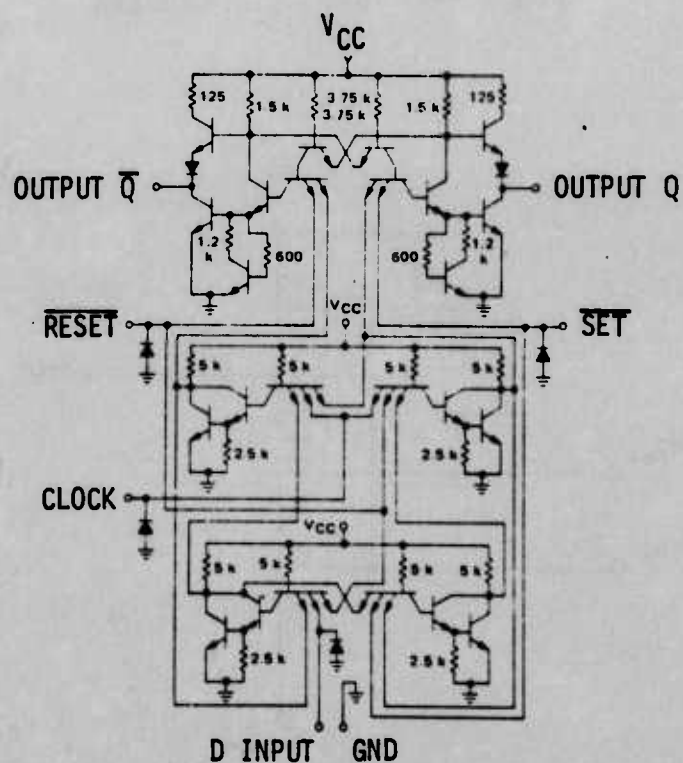


FIGURE E-4 7479 CIRCUIT DIAGRAM

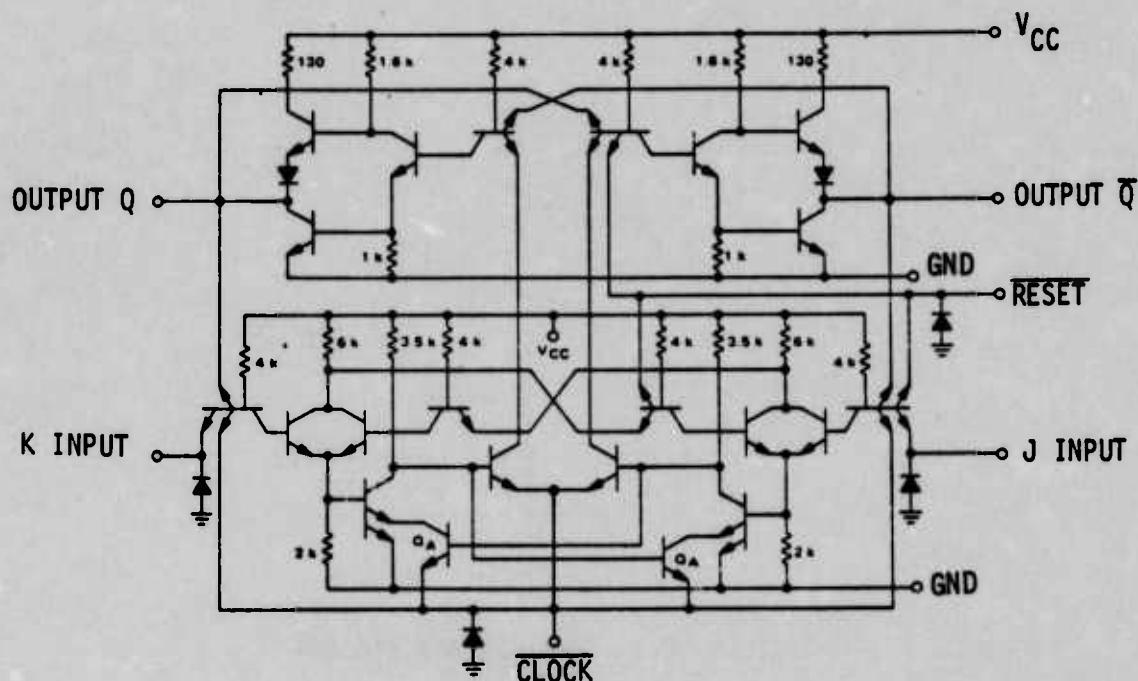


FIGURE E-5 7473 CIRCUIT DIAGRAM

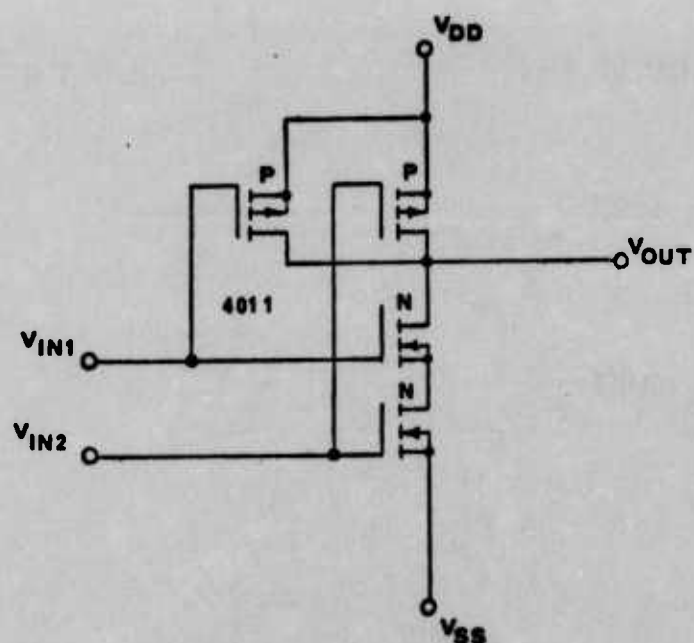


FIGURE E-6 4011 CIRCUIT DIAGRAM

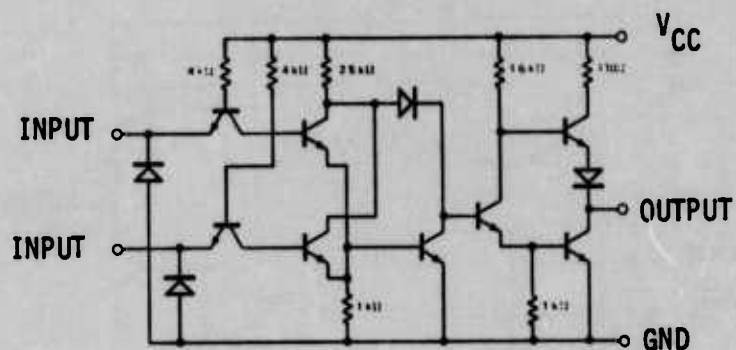


FIGURE E-7 7432 CIRCUIT DIAGRAM

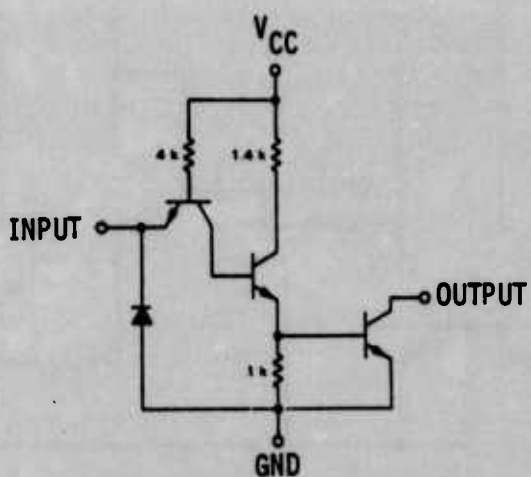


FIGURE E-8 7405 CIRCUIT DIAGRAM

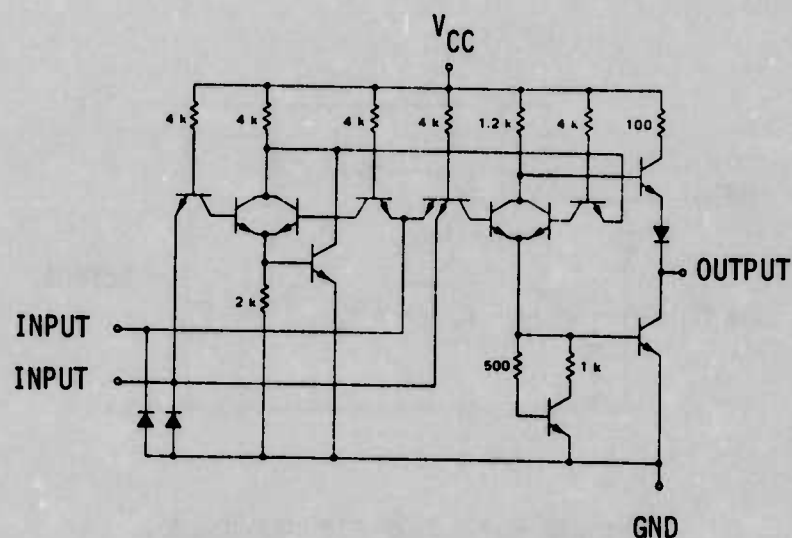


FIGURE E-9 3021 CIRCUIT DIAGRAM

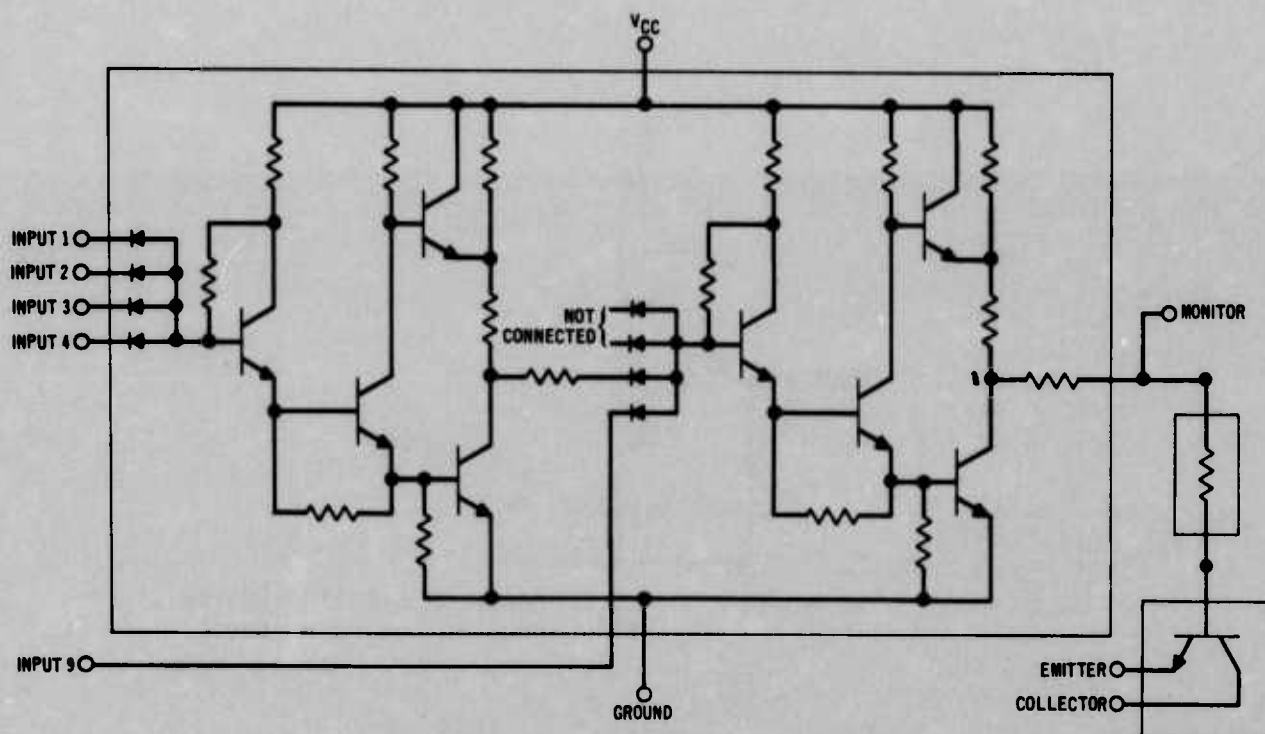


FIGURE E-10 2002 CIRCUIT DIAGRAM

INTEGRATED CIRCUIT SUSCEPTIBILITY

MDC E1126
9 AUGUST 1974

DISTRIBUTION

Executive Officer of the President
Office of Telecommunications Policy
Washington, D. C. 20504

ODDR&E
Assistant Director (E&PS)
Attn: Dr. George H. Heilmeier
Pentagon, Room 3D1079
Washington, D. C. 20301

Director, Defense Nuclear Agency
Attn: RAEV (Maj. W. Adams)
Washington, D. C. 20305

Chief of Naval Operations
Attn: OP-932
OP-932C
Washington, D. C. 20350

Chief of Naval Material
Attn: MAT-03423 (Lt. R. Birchfield)
PM7T
Washington, D. C. 20360

Headquarters, U. S. Air Force (RDPE)
Attn: Lt. Col. A. J. Bills
The Pentagon, Room 4D267
Washington, D. C. 20330

Commanding General, U. S. Army Electronics Command
Attn: AMSEL-TL-I (R. A. Gerhold)
HL-C (J. O'Neil)
Ft. Monmouth, New Jersey 07703

Commander, Naval Air Systems Command
Attn: AIR-360G (A. D. Klein)
Washington, D. C. 20360

Commander, Naval Electronic Systems Command
Attn: NAVELEX-095
NAVELEX-3041 (J. A. Cauffman)
NAVELEX-3044 (Navy Member: Advisory Group on Electron Devices,
Working Group on Low Power Devices)
NAVELEX-3108 (D. G. Sweet)
NAVELEX-5032 (C. W. Neill)
Washington, D. C. 20360

Commander, Naval Sea Systems Command
Attn: SEA-034
SEA-0341
SEA-06G
Washington, D. C. 20360

INTEGRATED CIRCUIT SUSCEPTIBILITY

MDC E1126
9 AUGUST 1974

Commander, Rome Air Development Center
Attn: RB (J. Scherer)
RBC1 (J. Smith)
RBC2 (H. Hewitt)
Griffiss Air Force Base
New York 13440

Commander, Air Force Avionics Laboratory
Attn: AFAL/TEA (H. H. Steenbergen)
Wright-Patterson A.F.B., Ohio 45433

Director, Avionics Engineering
Attn: EA (C. Seth)
Wright-Patterson A.F.B.
Dayton, Ohio 45433

Commander, Kirtland Air Force Base
Attn: AFWL/DYX (Dr. D. C. Wunsch)
New Mexico 87117

Commanding Officer, Harry Diamond Laboratory
Attn: J. Sweton
W. L. Vault
H. Dropkin
Washington, D. C. 20438

Commander, Naval Electronics Laboratory Center
Attn: Code 4800 (Dr. D. W. McQuitty)
(A. R. Hart)
San Diego, California 92152

Commander, Naval Ordnance Laboratory
Attn: Code 431 (Dr. M. Petree)
(Dr. J. Malloy)
(R. Haislmaier)

White Oak
Silver Springs, Maryland 20910

Commander, Naval Weapons Center
Attn: Code 5531 (D. Cobb)
Code 5535 (H. R. Blecha)
China Lake, California 93555

Reliability Analysis Center
Rome Air Development Center
Attn: RBRAC (I. Krulac)
Griffiss Air Force Base, New York 13441

Commanding Officer, Electromagnetic Compatibility
Analysis Center (ECAC)
Attn: CDR Case
J. Atkinson
North Severn
Annapolis, Maryland 21402

INTEGRATED CIRCUIT SUSCEPTIBILITY

MDC E1126
9 AUGUST 1974

Department of the Navy
Attn: Code 7624 (J. Ramsey)
Naval Ammunition Depot
Crane, Indiana 47522

Commander, Naval Electronics Systems Test and
Evaluation Facility
Attn: M. Gullberg
Webster Field
St. Inigoes, Maryland 20684

Naval Post Graduate School
Attn: Code AB (Dr. R. Adler)
Monterey, California 93940

National Bureau of Standards
Attn: J. French
H. Schafft
Washington, D. C. 20234

Dr. James Whalen, Room 2B
4232 Ridge Lea Road
State University of New York at Buffalo
Amherst, New York 14226

The Rand Corporation
Attn: A. L. Hiebert
1700 Main St.
Santa Monica, California 90406

Fairchild Research and Development
Attn: Dr. J. M. Early
M/S 30-0200
4001 Miranda Ave.
Palo Alto, California 94303

RCA Laboratories
Director, Solid State Technology Center
Attn: Dr. G. B. Herzog
Princeton, New Jersey 08540

Mr. J. S. Kilby
5924 Royal Lane
Suite 150
Dallas, Texas 75230

Dr. Gordon E. Moore, V.P.
Intel Corp.
3065 Bowers Road
Santa Clara, California 95051

INTEGRATED CIRCUIT SUSCEPTIBILITY

MDC E1126
9 AUGUST 1974

Bell Telephone Laboratories
Attn: Dr. G. E. Smith
Unipolar Design Department
600 Mountain Avenue
Murray Hill, New Jersey 07974

Automation Industries
Vitro Laboratories Division
Attn: T. H. Miller
14000 Georgia Ave.
Silver Springs, Maryland 20910

Braddock, Dunn, and McDonald, Inc.
Attn: J. Schwartz
First National Bank-East (17th Floor)
Albuquerque, New Mexico 87108

R&D Associates
Attn: Dr. W. Graham
P. O. Box 3480
Santa Monica, California 90406

Illinois Institute of Technology Research Institute
Attn: Dr. Weber
10 West 35th St.
Chicago, Illinois 60616

Research Triangle Institute
Attn: Dr. M. Simons
Dr. Burger
Research Triangle Park,
North Carolina 27709

Defense Documentation Center
Cameron Station
Alexandria, Virginia 22314

Secretariat, Advisory Group on Electron Devices
Attn: W. Kramer, Working Group B
201 Varick St.
New York, New York 10014

INTEGRATED CIRCUIT SUSCEPTIBILITY

MDC E1126
9 AUGUST 1974

LOCAL DISTRIBUTION

C

D

E

EPA/Hooker

F

FC

FE

FG

FV

FVE

FVN

FVR

G

GB

GBP

GBR

MIL

MIM